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DESIGN OF DIGITAL DOWN CONVERTER AND DIGITAL PREDISTORTOR FOR PREDISTORTION LINEARIZATED AMPLIFIERS

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Cette mémoire intitulée :

DESIGN OF DIGITAL DOWN CONVERTER AND DIGITAL PREDISTORTOR FOR PREDISTORTION LINEARIZATED AMPLIFIERS

présenté par : JING LI

En vue de l'obtention du diplôme de : MAITRISE EN SCIENCES APPLIQUEES

A été dûment accepté par le jury d'examen constitué de :

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DEDICATION

To my parents and my brother

To my daughter Weilu Wu

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First of all, I would like to express my sincere gratitude to my advisor, Professor Fadhel Ghannouchi, for his consistent direction, advice and encouragement during the course of my project.

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Abstract

Power amplifiers (PAs) in the third-generation (3G) wireless communication systems are becoming a bottleneck, which prevents the system to work in a high efficiency condition since the modulation scheme of the system requires very high linearity. Hence, various linearization methods have been presented to improve the linearity of the power amplifier so as to increase the efficiency of the communication system. The predistortion technique is one of the most promising linearization techniques, which is attracting attention of more and more researcher over the world. Taking advantage of high speed FPGA+DSP, the baseband digital predistortion is a cost-effective means with wide bandwidth and a superior linearization performance, and more, predistortion does not significantly compromise the efficiency of an amplifier.

The main objective of this thesis is to design a baseband digital predistortion system for linearizing RF power amplifiers of W-CDMA base station. In detail, the thesis concentrates on designing and implementing following modules: Baseband Digital Pre-Distorter (DPD), Dual-channel Mixer (down converter) and IF Amplifier, Digital Demodulator (DDEM).

At first, the characteristics of RF power amplifiers are summarized according to their bandwidth, output power, efficiency, and distortion performance. Different linearization techniques are reviewed and the focus is on discussing RF and baseband predistortion techniques and their implementation issues.

Then, a baseband DPD system is proposed. We describe the system architecture and the operation principle of each block in details. The factors such as the indexation companding function of Look-Up-Table (LUT), which strongly affect the predistortion performance is discussed. The simulation and parameter optimization of the DPD prototype was performed in Simulink (Mathworks).

After that, hardware requirements and implementation method of dual-channel receiver (Mixer + IF amplifier) are presented. The receiver was implemented with active mixer AD8343 and IF amplifier AD8370 from Analog Device Inc. The test results demonstrated that the receiver has high conversion gain and low distortion performance.

The digital logic circuit design of DPD and DDEM using Altera QuartusII software is presented. The design was optimized and implemented in Altera Stratix EP1S80 device. After that, the design was validated in Altera DSP development board. The predistortion outputs of the LUT were captured both in time and frequency domain. The measurement results are discussed in terms of the predistortion effectiveness.

Finally, we obtained a baseband DPD system with less complexity and high bandwidth, which was implemented in a FPGA device (Altera). This predistortion system exhibited good performance when it was applied to a practical power amplifier.

Résumé

Les amplificateurs de puissance utilisés dans les systèmes de communication sans fil de la troisième génération (3G) deviennent un goulot d'étranglement qui limite l'efficacité énergétique du système puisque les modulations employées exigent une très haute linéarité. Diverses méthodes de linéarisation ont été présentées afin d'améliorer la linéarité de l'amplificateur de puissance pour augmenter l'efficacité énergétique du système de communication. La technique de prédistorsion est l'une des techniques de linéarisation les plus prometteuses qui attire de plus en plus l'attention de chercheurs à travers le monde. En profitant de la haute vitesse des systèmes de traitement des signaux numériques tels que les réseaux de portes programmables (FPGA) et les processeurs de traitement des signaux numériques (DSP), la prédistorsion numérique en bande de base est un moyen rentable qui possède une large bande de correction et une bonne amélioration de la linéarité sans affecter l'efficacité énergétique de l'amplificateur.

Le principal objectif de ce mémoire est de concevoir un système de prédistorsion numérique en bande de base pour la linéarisation des amplificateurs de puissance RF des stations de base W-CDMA. En particulier, on se concentre sur l'implémentation de la fonction de prédistorsion ainsi que la conception et la réalisation du mélangeur à doubles canaux, des étages d'amplification intermédiaires et du démodulateur numérique.

Dans le premier chapitre, les caractéristiques des amplificateurs de puissance RF sont catégorisées selon leur largeur de bande, la puissance fournie, l'efficacité énergétique

et le niveau de distorsions. Ensuite, différentes techniques de linéarisation sont passées en revue, l'accent étant mis sur les techniques de prédistorsion en bande de base et leurs problèmes d'implémentation.

Dans la deuxième partie, on propose un nouveau système de prédistorsion numérique en bande de base. D'abord, l'architecture du système et le principe d'opération de chacun des blocs sont décrits. Ensuite, les facteurs tels que la fonction d'indexation de la table de correspondance, qui affecte fortement les performances du prédistordeur sont discutés. La simulation et l'optimisation des paramètres du prototype du prédistordeur ont été exécutées à l'aide du logiciel Simulink de Mathworks.

Dans la troisième partie, on a présenté les équipements requis et la méthode de réalisation du récepteur double canaux (le mélangeur et l'amplificateur fréquence intermédiaire) en utilisant le logiciel HP-ADS® de la compagnie Agilent. Le récepteur a été réalisé avec le mélangeur actif AD8343 et l'amplificateur fréquence intermédiaire AD8370 tous deux fabriqués par la compagnie Analog Devices. Les résultats de mesures démontrent que le récepteur a un gain de conversion élevé et génère un faible distorsion.

Finalement, on a présenté la conception du circuit numérique logique de prédistorsion et du démodulateur numérique à l'aide du logiciel Altera QuartusII. Le système a été optimisé et réalisé avec le dispositif Altera Stratix EP1S80. Ensuite, la conception a été validée à l'aide du circuit de développement Altera DSP. Les signaux prédistordus à la sortie de la table de correspondance ont été capturés dans les domaines de fréquence et du temps. Les résultats de mesures ont été discutés en termes de l'efficacité de la fonction de prédistorsion

Ainsi, nous avons réalisé, dans un dispositif FPGA, un système de prédistorsion numérique en bande de base moins complexe et possédant une bonne largeur de bande. La validation expérimentale de ce système de prédistorsion, appliqué à la linéarisation d'un amplificateur utilisé dans les stations de base dans le contexte des applications 3G, a montré de bonnes performances.

Condensé en Français

1. Introduction

Le système de communications sans fil W-CDMA est l'une des principales technologies cellulaires numériques à large bande qui sont utilisées pour 3G. Les amplificateurs de puissance (PAs) dans ce système, sont une partie importante de la chaîne de transmission qui doit répondre aux exigences de performance rigoureuses, et ce, afin de réaliser la spécification du système complet. Avec W-CDMA, le défi pour la conception consiste à maintenir la linéarité sur une bande passante large pour des signaux avec une grande valeur de crête.

En raison de l'enveloppe non constante des signaux W-CDMA, les exigences de linéarité des PAs sont très élevées, et un faible valeur du facteur n'est pas suffisante pour assurer cette linéarité, à cause de la mauvaise efficacité des PAs. Les techniques de linéarisation deviennent la seule façon possible de compenser les effets de distorsion et la dispersion spectrale causée par le nonlinéarité d'amplificateur près de la saturation. Des méthodes de linéarisation diverses ont été présentées, comme de correction en aval ou des techniques de pré distorsion. Parmi les approches proposées, la technique de prédistorsion est la plus prometteuse en raison de la largeur de bande. De plus, le prédistorsion ne réduit pas significativement l'efficacité d'un amplificateur.

Le circuit de prédistorsion est équivalent à un circuit non linéaire avec la réponse

d'expansion de gain qui est l'inverse de la réponse de compression de gain de PA et une réponse de phase qui est opposée à la réponse de phase PA. Les paramètres de correction de la prédistorsion inclus dans le LUT sont établis pour que l'équation suivante soit satisfaisante :

$$V_{out}(t) = f[P_d(t)]g[P_{in}(t)]V_{in}(t) = KV_{in}(t)$$

$P_{in}(t)$ Et $P_d(t)$ correspondant à la puissance instantanée des signaux à l'entrée et à la sortie du prédistorsion, f et g désignent respectivement les fonctions non linéaires de l'amplificateur de puissance et son prédistordeur correspondant qui dépendent de la puissance du signal d'entrée.

2. *Introduction de mise en oeuvre de système*

Le système est approprié pour des signaux W-CDMA et peut fonctionner, jusqu'à trois canaux de système de télécommunications mobiles universels et corrige les produits d'intermodulation d'ordre 3 etc.

Le système inclut la prédistorsion digitale (dans le FPGA), un canal à deux voies de conversion RF/IF, le démodulateur digital (dans le FPGA), basé sur des transistors Motorola-LDMOS de classe AB.

Le DPD est une partie clef du système. La prédistorsion numérique est conçue et à base d'une «Table de Correspondance» (LUT) et un multiplicateur complexe. Les valeurs de gain complexes la fonction de prédistorsion sont emmagasinées dans le LUT et indexées selon la puissance du signal d'entrée. Ce gain complexe représente la caractéristique du non-linéarité de l'amplificateur. La sortie LUT modifie le signal

d'entrée retardé au moyen d'un multiplicateur vectoriel, la déformation est ensuite appliquée au signal bande de base originale. L'équation de la fonction du multiplicateur vectoriel est :

$$I_p + jQ_p = (I_{in} + jQ_{in})(I_c + jQ_c) = (I_{in}I_c - Q_{in}Q_c) + j(I_{in}Q_c + I_cQ_{in})$$

Dans la rétroaction, il y a un récepteur de canal à deux voies, qui sert pour la transformer les signaux RF à l'entrée et à la sortie du PA aux fréquences intermédiaires. Le mélangeur a été conçu soigneusement pour obtenir la même fonction dans les deux voies qui est la base de la synthèse adaptative. Un convertisseur A/N (Analogique à Numérique) à deux voies, 12-bit et 125MSPs est utilisé pour numériser les signaux d'entrée analogiques des deux sorties des mélangeurs. Les deux signaux numérisés sont démodulés en utilisant le canal à deux voies et le démodulateur numérisé (DDEM) à change. Les caractéristiques dynamiques AM/AM et AM/PM de l'amplificateur sont construit en utilisant les enregistrements des composants Q et I, des signaux à l'entrée et à la sortie. Basé sur ces caractéristiques non linéaires du PA, les entrées LUT sont directement synthétisées en utilisant le processeur DSP.

La conception du DPD et DDEM est basée sur des oscillateurs numériquement contrôlés (NCOs), des filtres FIR, des blocs DSP, un interpolateur et quelques de circuits logiques d'assemblage. Le dispositif cible est le EPS1S80B956C6 sur le tableau de développement Stratix EP1S80 DSP d'Altera. Le logiciel de développement de conception comprend un environnement de simulation de système MATLAB, l'environnement de conception VHDL, QuartusII 4.0 d'Altera. Le récepteur de canal à

deux voies consiste en un mélangeur et un amplificateur. Le mélangeur représente un avertisseur abaisseur de fréquence de la RF l'IF, l'amplificateur IF fournit la tension nécessaire pour le convertisseur A/N. Les circuits d'Analog Device : AD8343 et AD8370 ont été utilisés comme dispositifs principaux du mélangeur et de l'amplificateur IF respectivement.

3. *La conception et la mise en oeuvre du mélangeur*

La multiplication est mélangeur de fréquence; le multiplicateur idéal ferait un mélangeur excellent. La théorie est exprimée dans l'identité trigonométrique suivante :

$$\sin(w_{sig}t)\sin(w_{LO}t) = 1/2\{\cos(w_{sig}t - w_{LO}t) - \cos(w_{sig}t + w_{LO}t)\}$$

Le convertisseur abaisseur de fréquences sont le signal dont les fréquences est la différence des fréquences multipliée. La conversion de fréquence arrive suite à la multiplication du signal par un signal carré à la fréquence de LO. La sortie du mélangeur contiendra donc des signaux $F_{LO} \pm F_{sig}$, $3F_{LO} \pm F_{sig}$, $5F_{LO} \pm F_{sig}$ et $7F_{LO} \pm F_{sig}$.

Comparé au mélangeur traditionnel passif, la linéarité élevée bien conçue des mélangeurs actifs offre des avantages attirants : Les bas niveaux de l'oscillatoire et de fuite, un niveau de signal de sortie plus haut et une taille plus petite. Basé sur ces caractéristiques principales, nous avons choisi le AD8343 d'Analog Devices comme dispositif principal utilisé dans le mélangeur, en raison de son gain élevé (7.1dB), de son large de bande passante (jusqu'à 2.5GHz), et des valeurs faibles des produits d'intermodulation et du facteur de bruit.

Les composants du mélangeur sont : le dispositif de mélangeur principal AD8343, l'interface d'entrée et le circuit d'adaptation, l'interface de sortie et le circuit de polarisation en puissance. Le mélangeur utilise un LO externe avec le niveau d'entrée de –10dBm, le AD8343 à l'entrée différentielle, la sortie et l'interface de LO pour une meilleure performance d'inter modulation.

Parce que l'entrée le signal RF différentielle avec la fréquence d'opération autour 2.0GHz, un réseau d'adaptation d'impédance approprié est l'élément clef dans la conception. La conception du réseau d'adaptation d'entrée comporte deux buts : adapter d'impédance de la source à l'impédance d'entrée de l'AD8343 et fournir continue de polarisation pour les résistances. La conception de circuit d'adaptation se réalise avec l'équivalent différentiel du classique en"L", le réseau est conçu en utilisant des valeurs d'un réseau différentiel, converti ensuite en différentiel.

Au moyen d'un analyseur de réseau vectoriel à deux ports VNA et de Agilent ADS, une mesure des paramètres S à l'entrée et la conception du circuit d'adaptation d'entrée a été réalisée utilisant les techniques d'adaptation d'impédance standard. Le mélangeur exige une entrée RF, une entrée LO et une sortie IF. Les transformateurs utilisés dans ces interfaces pour réaliser la conversion de terminaison différentielle à simple sont désirables et fournissent une linéarité élevée, une bonne isolation de sortie LO et une bonne isolation entre l'entrée et le sortie.

Finalement un filtre passe-bas est utilisé pour rejeter les hautes fréquences indésirables dans la conversion de fréquence en multipliant par un signal carré à la fréquence de LO.

Le PCB du mélangeur a été conçu avec le logiciel ProtelXP. Le substrat utilisé est le RO3006.

La mise en oeuvre du mélangeur inclut deux parties : premièrement une carte simple canal; configurée pour faciliter les mesures d'impédances faites dans le processus de conception des circuits d'adaptation pour l'application finale. La deuxième carte à double canal est conçue pour faire fonctionner l'AD8343 dans un environnement différentiel et inclut donc deux canaux tant dans l'entrée que dans la sortie du PA.

Les résultats de mesure ont démontré plus que 5.5dB de gain, 56.9dBc de performance d'inter modulation, un fonctionnement à large bande à 2.0GHz et la variation de gain inférieur à 0.5dB sur toute la bande d'opération.

4. Conception et mise en œuvre de l'amplificateur IF

L'amplificateur IF est un amplificateur de conducteur de condition entre le mélangeur et le convertisseur A/N, il fournit un gain réglable, et un niveau élevé de puissance pour alimenter le convertisseur A/N. Le dispositif principal utilisé dans l'amplificateur IF est le AD8370 d'Analog Device. Le AD8370 est un amplificateur à gain variable numériquement contrôlé. Il offre un contrôle de gain précise entre +6dB et +34dB utilisant l'interface digitale de 8-bit périodiques, un IP3 élevé de +35dBm à 70MHz, un faible facteur de bruit.

L'amplificateur IF inclut un amplificateur principal AD8370, un filtre passe-bas SCLF-65 avec une fréquence de coupure égale à 60MHz, un transformateur d'entrée TC4-1T, un transformateur de sortie TC2-1T et le circuit de polarisation et de couplage.

La mesure de la carte est basée sur le mélangeur à un seul canal + l'amplificateur IF, des résultats ont plus de 20dB de gain, 61.3dBc de performance d'inter modulation, moins de 0.5dB de variation de gain dans la gamme de fréquence de 1.5MHz - 60MHz.

5. Mise en œuvre et conception de DPD et DDEM utilisant FPGA

Au moyen de la plate forme de conception matérielle DSP d'Altera (le Kit de Développement DSP), les DPD et DDEM sont conçus et mis en oeuvre dans le FPGA. Le logiciel QuartusII fournit un environnement logiciel complet pour mettre en oeuvre la conception matérielle du circuit. Le Stratix DSP fournit une plate-forme de vérification. Le dispositif Stratix EPS1S80B956C6 d'Altera est le dispositif cible de conception.

Il y a plusieurs avantages de mettre en oeuvre le DPD et la conception du DDEM dans le domaine numérique utilisant la technologie de traitant numérique du signal:

- Cela permet une plus grande flexibilité et une performance supérieure en termes d'atténuation et de sélectivité.
- Offre un temps et une stabilité d'environnement meilleur que ceux offerts par techniques analogiques traditionnelles.
- Les composantes disponibles ultra rapides font que le DSP peut s'étendre de la bande large aux fréquences intermédiaires; le DSP est utile pour accorder le choix du signal, la fréquence de conversion élevée et basse.

Démodulateur Digital

Le DDEM transforme le signal IF large bande à un signal bande de base par une

multiplication en quadrature. Le NCO produit des signaux sinusoïdaux en quadrature pour les multiplicateurs. Le signal à bande de base complexe est filtré par un filtre pour empêcher le repliement de spectre aux fréquences harmoniques.

La conception du DDEM utilise deux fonctions propriétés intellectuelles Altera(IP) : Compilateur de Réponse Impulsionnelle Finie (FIR), compilateur oscillateurs d'un Numériquement Contrôlés (NCO). La conception est basée sur une opération fractionnelle à point fixe avec une précision limitée.

Le Compilateur NCO est utilisé pour produire la fréquence 30.72MHz à une fréquence d'échantillonnage de 122.88MHz sous formes de sinus et de cosinus pour les deux canaux Q et I. Avec les paramètres associés, le traceur spectral intégré montre que NCO fournit 106.2dB, comme rapport signal à bruit de quantification, à la précision de production de 18-bit à la sortie soit une résolution de fréquence 0.05722Hz.

La mise en oeuvre du DDEM emploie 2 multiplications à 122.88MHz, le multiplicateur accepte des données à IF de 14-bit à l'entrée et de NCO 18–bit à l'entrée et en résulte 14-bit pour une sortie de précision limitée.

Le compilateur FIR forme un filtre passe-bas afin de filtrer les fréquences images. Le filtre utilise une structure 45 taps Blackman avec des fréquences de coupure 15.36MHz, et fournit une réjection de 80dB.

Prédistorsion digitale

La conception d'une predistortion numérique consiste en trois blocs principaux: Deux filtres à une interpolation de 4 fois (4X_FIR), un Table de Correspondance (LUT)

et un Multiplicateur Vectoriel (V_MULT).

a) **Interpolateur 4X_FIR** augmente le taux d'échantillons à la sortie d'un facteur de 4 par l'insertion de 3 zéros entre des échantillons d'entrée et augmente la fréquence d'échantillonnage de 30.72MSPs à 122.88MSPs. L'interpolateur peut augmenter la fréquence d'échantillonnage à l'entrée, alors si la nouvelle fréquence Nyquist est plus haute, l'espace entre le signal désiré et la fréquence repliée est-elle aussi plus haute et diminue les contraintes requises sur le filtre passe-bas analogique à la sortie du convertisseur N/A. Un filtre interpolateur est mis en oeuvre avec l'architecture polyphasé en utilisant l'architecture multi-cycle variable du compilateur FIR. L'interpolation est exécutée en deux étapes l'échantillonnage et le filtrage quart-bande pour filtrer les images introduites par l'insertion de zéros. La performance de l'interpolation est évaluée dans le domaine de fréquence et les spectres de signal de sortie du convertisseur N/A consistent en la fondamental et les harmoniques à la fréquence $\pm I * 30.72MHz$ (I est le facteur d'interpolation), c'est claire que l'augmentation du facteur d'interpolation augmente l'espacement entre la fondamental et les harmoniques

b) **Look Up Table (LUT)** inclut un bloc de calcul d'adresse du tableaux $I^2 + Q^2$ et deux tableaux qui sont construits utilisant deux port RAM (2*2048bits). Un multiplieur additionneur/accumulateur, qui met en oeuvre le calcul d'adresse de table, tant à l'entrée qu'à la sortie à une précision limitée à 14-bit. La Mégafonction paramétrée de la RAM deux ports crée les tables Q et I avec le fichier d'initialisation de mémoire, chaque mémoire à une profondeur de 2048 et une largeurs de14-bit.

c) **Multiplieur Vectoriel** : Deux multiplieurs/accumulateurs mettent en oeuvre le sous block du multiplieur vectoriel. L'utilisation d'un seul block DSP (quatre 18-bit x 18-bit) permet la mise en œuvre des deux multiplieurs/accumulateurs avec addition et soustraction. La partie réelle $I_p = I_{in}I_c - Q_{in}Q_c$ utilise un multiplier avec un accumulateur/soustracteur et la partie imaginaire $Q_p = I_{in}Q_c + I_cQ_{in}$ utilise un multiplier avec accumulateur additionneur. Les deux opérations ont une précision limitée de 14-bit.

La conception du DPD est validée dans la carte de développement Stratix d'Altera, les résultats de mesures dans le domaine temps et fréquence montrait la performance du prédistorteur quand on applique un signal 3G, qui coïncident avec résultats de la simulation dans Matlab Simulink.

6. Conclusion

La mise en oeuvre du DPD et du DDEM est basée sur une architecture modulaire, rapide et flexible prototypage, une précision au niveau bit et une performance supérieure : La vitesse du traitement numérique jusqu'à 150MHz peuvent de supporte jusqu'à 50MHz de largeur de bande.

Un mélangeur actif et un amplificateur IF sont bien conçus utilisant une architecture balancée flexible et simple, Ils ont démontré de bonnes performances : bruit et intermodulation faible, un gain de conversion élevé, une faible puissance nécessaire pour le signal LO. Une symétrie presque parfaite du lay-out du circuit a comme conséquence la basse fuite RF et LO. Les résultats de mesure montrent un gain supérieur

à 20dB et 61.3dBc d'intermodulation.

L'amplificateur linearise avec son nouveau DPD et le récepteur de double canal d'améliorer les performances de la linéarisation, ceci peut aboutir à un produit avec de bonnes performances: Large bande d'opération, une bonne linéarité, une simplicité de mise en œuvre dans un future proche. L'amélioration de performances résulte de la nouvelle approche de conception a mélangé RF/DSP+FPGA.

Table of Contents

List of Tables

List of Figures

Abbreviations and Acronyms

3G	Third Generation
ADC	Analog to Digital Converter
ACPR	Adjacent Channel Power Ratios
DAC	Digital to Analog Converter
DDEM	Digital Demodulator
DPD	Digital Pre-Distortion
DSP	Digital Signal Processing
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile communications
IF	Intermediates Frequencies
IMD	Intermodulation Distortion
IS-95	Digital Cellular Standard IS-95
IP3	Third-order Intercepts Point
LINC	Linear Amplification Using Nonlinear Components
LO	Local Oscillator
LSB	Least Significant Bit
LUT	Look Up Table
MAC	Multiply Accumulate

MSB	Most Significant Bit
NCO	Numerically Controlled Oscillator
PAR	Peak-to-Average power Ratios
PLL	Phase Locked Loops
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SNR	Signal to Noise Ratio
VMOD	Vector Modulator
W-CDMA	Wideband Code Division Multiple Access

Chapter 1: Review of Digital Predistortion

1.1. Introduction

While the third generation (3G) of mobile radio standards for mobile communication systems and wireless multimedia services are being defined, the quantity and complexity of the signals to be transmitted is increasing. The demands placed on radio frequency power amplifiers, which are used in such system, are increasing in terms of bandwidth, output power, efficiency, and performance of output distortion. There is growing need for amplifiers, which amplify all types of signals without adding significant distortion and that are capable of operating over a wide bandwidth and at high levels of output power.

W-CDMA is one of the leading wideband digital cellular technologies that will be used for 3G applications. Power amplifiers (PAs) in a W-CDMA are a key part of the transmit chain, and have to meet rigorous performance requirements in order to achieve the overall system specification. With W-CDMA, the challenge for designing PAs is to maintain linearity over a wider bandwidth, while at the same time supporting high peak-to-average ratios [1].

1.2. Linearization requirements for PAs and technological review

Due to the non-constant envelope of W-CDMA signals, the linearity requirements of the PAs are very high, a simple back off is not feasible to achieve the required linearity

because of resulting poor PA efficiency. Traditionally, the approach has been to use linear amplifiers, such as class-A amplifiers, and to operate it in the linear mode by backing off from the saturation range, thereby compromising the efficiency of the system. This results in excessive power consumption as well as high equipment costs, which in some cases run up to 1/3 of the overall base-station cost.

The application of more efficient amplifiers such as class-AB or class-C PAs is a viable alternative to low efficiency linear amplifiers. But degradation of linearity becomes significant as the PA operates close to saturation where both high power efficiency and high output power emission are achieved. Figure1-1 shows the typical PA response of a Class-AB RF high power amplifier.

Linearization techniques become the only possible way to compensate the distortion effects and spectral spreading caused by the amplifier non-linearity.

Various linearization methods have been reported and are derived, in general, there are three main types, and which can be categorized as:

1) Feedback: Feedback is applied for limited bandwidth capability and has a potential instability; this is not suitable for W-CDMA signals because of the fast variation of the envelope and the fast power control required.

2) Feedforward: This linearization concept works at RF. It is used when a high level of linearity and a wide bandwidth are needed. The main disadvantage of this concept is the high back off for the error amplifier (auxiliary amplifier), which reduces the maximum achievable efficiency to 10...15%. The implementation is also complicated and expensive.

3) Predistortion: It works at RF or baseband, the linearity improvement is evident to third order distortions, and it has good efficiency. It is easy to implement in the digital domain.

4) LINC (Linear Amplification Using Nonlinear Components): It has good linearity and high efficiency performance, but suffers from some constraints regarding of implementation, such as signal combining losses.

Feedback and RF synthesis (LINC) are presented as examples of narrowband schemes, while predistortion and feedforward are suitable for wideband systems. Table 1 shows the performance comparison of linearization techniques.

Table 1 Linearization technique comparison

Correction Technologies	Correction Capability	Correction Bandwidth	Relative Cost
Feed Forward	25-35 dB	> 100 MHz	High
Envelope Feedback	10-20 dB	< 5 MHz	Med
Analog Predistortion	5-10 dB	> 25 MHz	Low
Digital Predistortion	10-20 dB	> 50 MHz	Med

To evaluate linearization performance of PAs for 3GPP, there are several important performance factors that can be specified and measured. The following sections describe some key specifications characterizing the performance of these RF PAs.

- Adjacent channel interference

ACPR is an important measure of transmitter performance. It is defined as the

ratio of the transmitted power to adjacent RF channels the power. The main source of adjacent channel leakage is due to nonlinear effects in the power amplifiers. The current values in the 3GPP requirements for the BTS are 45dB at 5MHz offset and 50dB at 10MHz offset.

- Handling high Peak-to-Average power Ratios (PAR) & Efficiency

Some 2G system, such as GSM, use a constant modulation format (GMSK), it has the advantage of a constant amplitude envelope, which allows the use of less expensive, non-linear Class-B PAs. By contrast, CDMA use non-constant modulation formats (QPSK and QAM).

PAR is the ratio of the peak envelope power to the average envelope power of the signal. Moreover, in CDMA systems, as multiple channels are added to a single carrier, the PAR increases as code channels are activated. The use of multi-carrier is similar, peaks occur when individual carriers (codes) are phase aligned.

The amplifier must be capable of handling the high PAR that the signal exhibits, while at the same time maintaining good ACPR performances. This all pushes the design complexity of PAs one-step further.

In practice, high PAR and efficiency cannot be obtained simultaneously. For example, for a multicarrier signal having an envelope that has a Rayleigh distribution. The amplitude density function is given by [3]

$$f(v) = 2\mu v e^{-\mu v^2} \tag{1.1}$$

If the peak voltage is unity, PAR is μ, for each envelope amplitude $0 \le v \le 1$,

Class-A and Class-AB power amplifiers the efficiency is theoretically:

$$\eta_{Class-AB} = \sqrt{\frac{\pi}{4\mu}} \tag{1.2}$$

$$\eta_{Class-A} = \frac{1}{2\mu} \tag{1.3}$$

The exact operating point of a transistor in terms of the class of operation is a compromise between linearity and efficiency. Increasing the bias current for better linearity (close to Class A operation) results in lower efficiency and more heat dissipation. Alternatively, lowering the bias current to improve efficiency (closer to Class B) results in reduced linearity.

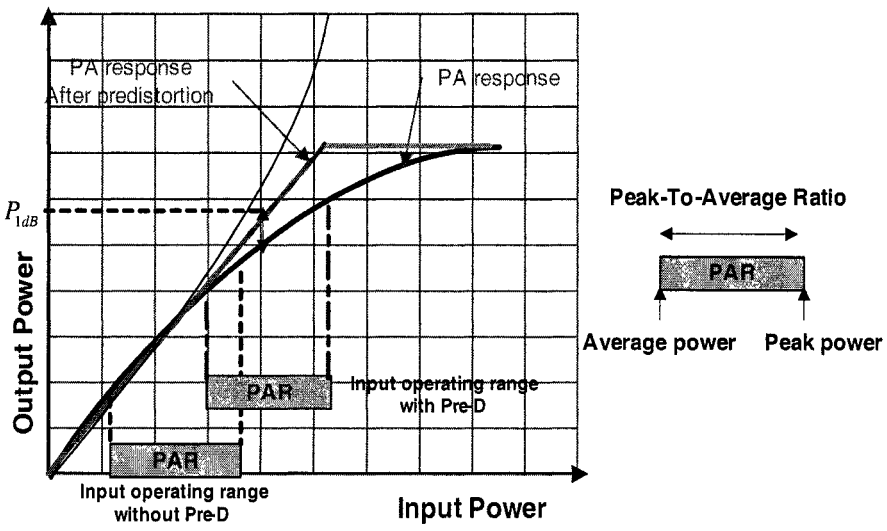

Figure 1- 1 Input and output response of a Class-AB RF power amplifier

- Two-tone test --- Harmonic and intermodulation distortion of PAs

The particularities of nonconstant envelope behavior make the two-tone test a very

useful test and measurement too since the amplifier is driven through the whole range of its transfer characteristic.

Consider two tones of equal amplitude have frequency and respectively:

$$V_{in} = a\cos(2\pi f_1 t) + a\cos(2\pi f_2 t) \tag{1.4}$$

For the nonlinear output, the Fourier transform representation of the distorted signal is shown in figure1-2. In addition to harmonic distortion, other frequency components or intermodulation (IM) products, are also present a DC term, fundamental tones and -compressed, harmonics, intermodulation products. If the input signal level is increased by 1dB, the second-order terms increase by 2dB (proportional to a^2), and the third –order terms increase by 3dB (proportional to a^3).

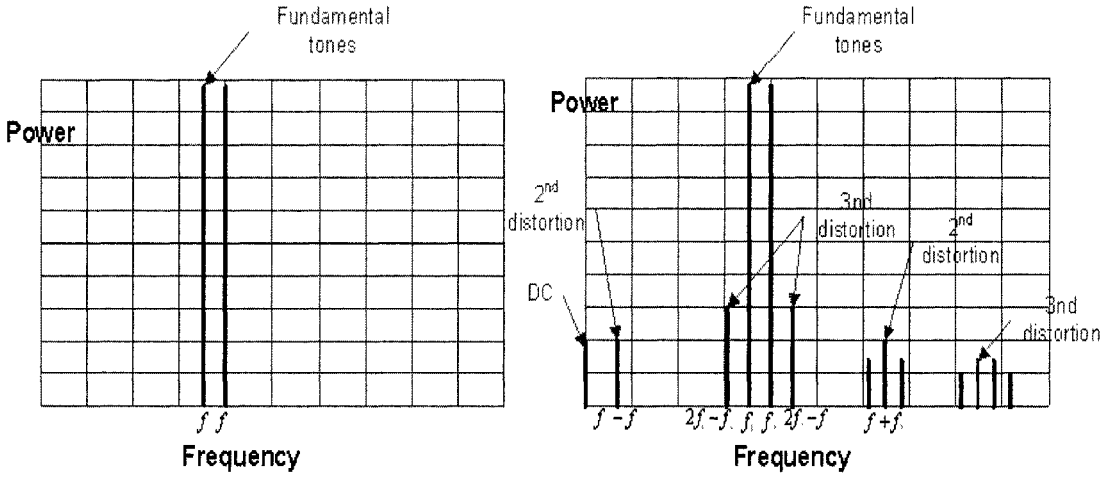

Figure 1- 2 Two-tone input and nonlinear output

- Third-order intercepts point IP3 and gain compression point P_{1dB}

The terms $\cos(2w_1 - w_2)$ and $\cos(2w_2 - w_1)$ are often used due to their closeness

to the fundamental signal. They are proportional to a^3. These intermodulation products increase by 3dB when the fundamental goes up by 1dB. The IP3 is defined as the theoretical level at which the third order intermodulation products are equal in power to the fundamental tone.

The output of an amplifier compresses at high signal levels (figure1-1) that is the gain drops. The 1-dB compression point P_{1dB} is the output power level at which the gain has dropped by 1dB compared to the linear region. P_{1dB} is used as a figure of merit in Class-B and Class-AB amplifiers. The IP3 is approximately 10dB above the gain compression point both analytically and experimentally [4]:

$$P_{IP3}(dBm) = P_{1dB}(dBm) + 10(dB) \tag{1.5}$$

1.3. Predistortion linearization technology

The predistortion technique is the most common method due to its wide bandwidth. Moreover, predistortion does not significantly compromise the efficiency of an amplifier.

The predistortion technique has historically been implemented using analog technique. Now this technique is well suited to digital implementation by integrating FPGA and DSP techniques to handle high-speed arithmetic. Predistortion based on FPGA+DSP techniques is a cost-effective means of compensating for PA nonlinearity and retaining efficiency. Predistortion implementation in DSP+FPGA has advantages compared to analog implementations; it reduces complexity, facilitates high integration,

improves efficiency and has superior performance.

The principle of predistortion is by introducing of a nonlinearity, which has the inverse of the amplifier's transfer characteristic in order to compensate for the amplifier distortion. The predistortion circuit is equivalent to a nonlinear circuit with a gain expansion response that is the inverse of the PA's gain compression response, and a phase response that is the negative of the PA's phase response.

In the view of signal processing technology, there are two types of predistortion compensation methods: one using an analog signal to provide the distortion, and the other using a digital signal to provide the distortion.

The predistorter can be implemented at baseband or RF. Both can use digital signal distortion methods.

For the compensation technique, there are data predistortion compensation techniques and signal predistortion compensation technique. The data predistortion technique attempts only to distort the transmitted code information data. In other words, the shape of the input signals constellation is modified. This only compensates the in-band distortion at the sampling instant and does not eliminate the out-of-band distortion. This technique is related to modulation type. The signal predistortion compensation technique distorts oversampled signal waveforms instead of the data constellation itself. It can eliminate the distortion both in-band and out-of-band. Both baseband and RF predistortion can make use of the signal predistortion compensation technique.

Predistortion can correct for both AM/AM and AM/PM distortion and is not restricted in bandwidth since there is no inherent feedback path. However, the adaptive

predistortion are bandwidth limited due to the DSP processor speed. Fixed or adaptive predistortion schemes can be used. Adaptive predistortion can compensate for changes in the amplifier characteristics over time, due to temperature and age, for example.

Fixed predistortion can be implemented based on a Look-Up-Table (LUT) or a polynomial work function. For the LUT approach, the complex gain values of the predistorter are stored in RAM and are dependant on the input signal amplitude or power. The work function approach applies the approximate nonlinear curve of the amplifier, by training the coefficients of the curve, by using the error of the gain and phase response, and then adjusting the parameters of the inverse function.

Adaptative predistortion algorithms based on the LUT are implemented on a DSP processor platform.

Baseband predistortion methods are suitable only when the baseband signal is directly accessible before up-conversion. It has moderate bandwidth and good relative IMD correction. Sometime it is limited by the DSP's computational capability, however in recent years the baseband predistortion technique has taken precedence due to the advances in high-speed digital signal processing (DSP) and field programmable gate array (FPGA) technology. In some cases, linearization designers have no access to the baseband signal, and are confined to RF envelope predistortion techniques.

It is possible, using both techniques to meet severe ACPR requirements despite high crest factor, high back off and large bandwidth requirement. Both predistortion technologies are perceived to be the most suitable and cost-effective linearization technique in the context of 3G wireless signals.

1.4. RF/Envelope digital predistortion

RF predistortion technology using look-up-table (LUT) operates well independently from the baseband block and generally follow power-control.

The architectures of RF/Envelope digital predistorter is based on an RF input signal. It is actually a hybrid predistortion method (analog and digital) because the envelope processing is digital in the baseband field. It uses a RF vector modulator (Vector Multiplier); the predistortion information (AM/AM and AM/PM based on instantaneous PA characterization) is applied to a complex gain tuning circuit that controls the amplitude and phase of the RF signal. Figure1-3 shows the architecture diagram of an RF/Envelope DPD implementation [5] [9] [24] [25].

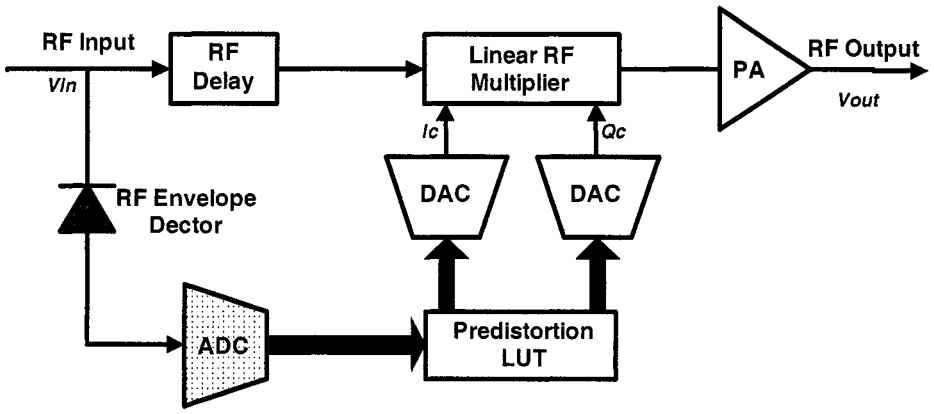

Figure 1- 3 RF/envelope DPD architecture block diagram

RF linear vector multiplier is a key-component in the predistorter. It adjusts the input signal magnitude and phases through a multiplication with the correction parameters I_c and Q_c recorded in the LUT. Considering the variable envelope of the

input signal, which is already modulated, a simple vector modulator doesn't allow a linear multiplication operation according to I_c and Q_c along with the input signal magnitude. Predistortion correction parameters in the LUT are determined so that equation (1.6) is satisfied [5].

$$V_{out}(t) = f[P_d(t)]g[P_{in}(t)]V_{in}(t) = KV_{in}(t) \tag{1.6}$$

$P_{in}(t)$ and $P_d(t)$ correspond to the instantaneous power of the signals at the input and output of the predistorter. K is the linear gain of the PA. The nonlinear functions of the power amplifier and its corresponding predistorter are designated by f and g respectively, which depend on the input signal power.

However, in this envelope predistortion system, an Envelope Detector, a Vector Modulator (VMOD) and filters include nonlinear components. These nonlinear characteristics lower the effects of linearization and should be compensated for. VMOD for example, suffers from several deficiencies, such as amplitude and phase imbalance and DC offset. Compensation for these impairments is needed, and increases the complexity of the circuit.

A precise determination of the group-delays of each path, in the predistortion loop is required for the compensation for any delay imbalance that could compromise the linearization. At each instant, correction parameters I_c and Q_c must be available to the input of the linear RF vector multiplier at the same time as the corresponding samples of passed input signal, and the problem of delay that pass through Detector, ADC, FPGA, DAC, and VMOD is tedious and almost impossible to compensate for in the RF path.

1.5. Adaptive baseband digital predistortion

Another predistortion approach is baseband digital predistortion, which is based on orthogonal baseband digital I/Q data stream. The general architecture for a system with baseband DPD is shown in figure 1-4. Because the predistortion is implemented in baseband and the distorted signal is up converted to RF, there are no comparable group-delays between the baseband path and the RF path that need to be compensated. And all the predistortion processing can be handled in digital domain [7] [10].

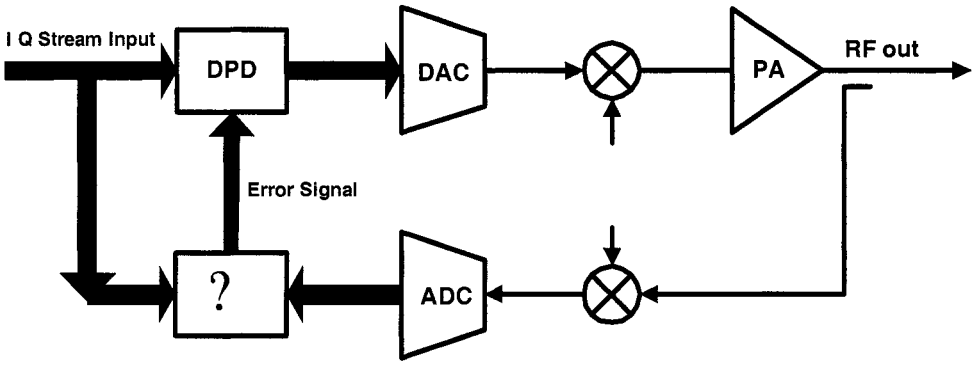

Figure 1- 4 Baseband DPD architecture block diagram

The implementation of the digital predistorter is also a look-up-table with complex correction/modification values for each complex sample of the input signal. This LUT would allow more flexibility for the approximation of the nonlinear characteristics of the power amplifier.

The predistorter manipulates the signal in baseband to minimize the nonlinearity in the output of the amplifier by applying the inverted nonlinearity (generated by the amplifier) to input I/Q signals; this leads to an increased requirement in digital signal

processing speed with the required high bandwidth (multi-carrier W-CDMA) signal.

Because of time-variant effects (temperature, load, supply-voltage...) the nonlinearity (AM-AM, AM-PM) of the amplifier must be measured during operation to adapt the predistortion characteristics into the table. In order to understand and optimize the distortion compensation, a circuit is installed to provide feedback on the status of the post-amplified signal. By setting a demodulator in the feedback loop, distortion compensation optimization can be strictly planned and deal with according to changes in characteristics. Updating distortion compensation focuses on minimizing the spectrum distortion emission of the output signal of the PA, which means that if the linearity is not sufficient, the coefficients and parameters of the predistorter must be modified to achieve a higher linearity.

In the above-mentioned approach, by taking advantage of the increasing processing speed in ADC, DAC and FPGA+DSP, we can archive wider bandwidth. But memory effects have to be taken into account, which limits its use in linearization as bandwidth increased.

Chapter 2: DPD System Implementation Prototype

2.1 Introduction

The baseband predistorter and the IF demodulator are the critical parts in the predistortion system. They are implemented in the digital domain. The FPGA is a superior platform for the implementation of a digital demodulator and a digital predistorter.

1) The FPGA with its field programmability offers scalability for using in highly integrated solution. They can integrate DDC (Digital Down Converter), DPD, Resample Data Reformatting as well as a DSP processor into a single chip. FPGA-based implementations offer a System-on-Chip solutions.

2) The FPGA offers better time and environment stability than traditional analog techniques.

3) They afford greater flexibility and higher performance in terms of signal attenuation and selectivity.

By combining drop-in intellectual property (IP) with FPGA devices, Altera DSP Development Kit, Stratix Professional Edition provides both a design and experimental platforms. The DPD and DDEM designs consist of Numerically Controlled Oscillators (NCO), FIR, and DSP blocks. The target device is the Stratix EPS1S80B956C6. The design development software comprises a MATLAB system simulation environment, Altera QuartusII 4.0 design software, and VHDL design language.

2.2 *System description*

The system includes a baseband digital predistorter (in FPGA), a dual-channel RF to IF Down Converter (Mixer), a dual-channel Digital Demodulator (in FPGA), a 90-W peak power amplifier based on Motorola-LDMOS class-AB transistors. Predistortion adaptive algorithm is implemented in DSP embedded processor (ADI Tiger Sharc).

The LUT addresses are derived from the input signal power. The LUT contains two values: The real part I and imaginary part Q. The predistorted baseband signal is modulated and upconverted to the PA. The PA output is down converted and measured. The error between predistorted output and the PA output is derived. Delay blocks ensure that the input is compared to the correct output value. The error signal is then used to update the values currently stored in the LUT. These updated values reflect changes in the PA behaviors over time due to ageing and temperature.

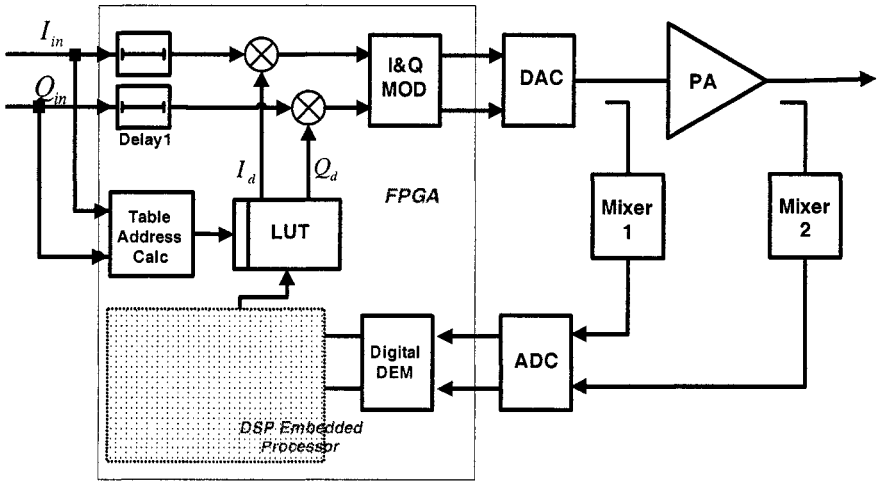

Figure 2- 1 Baseband DPD implementation architecture diagram

2.3 *Digital predistorter*

First the input baseband signal is fed into the index calculation block for determining the entries (address) of the LUT. The LUT output modifies the delayed input data by means of a vector multiplier, and then is applied to original baseband signal. The power of the input signal determines the LUT address. We can also utilize other indexing schemes such as magnitude, log or other nonuniform index companding algorithms.

The input data is delayed by the Delay1 blocks prior to undergoing a complex multiplication with the value read from the LUT in order to compensate for the delay through the index calculation block and reading out of data from the LUT.

The input data Q and I has a bus of 14 bits and being is fed to the index calculation block, which determines the address of the LUT. The indexing function of the LUT can seriously affect the efficiency of the system. Indexing with the power ($I^2 + Q^2$) causes table entries to be denser and in larger amplitude. Indexing with the amplitude of input signal ($\sqrt{I^2 + Q^2}$) leads to equal spacing of LUT entries in the amplitude domain. Non-uniform spacing, in which table entries are closely spaced where the amplifier characteristics vary sharply, provides better performance [6] [11] [12].

The key to implementing indexing of the LUT is in the companding function $C_{function}\{P(t)\}$ inserted between the calculation of input power $P(t) = I^2 + Q^2$ and the index variable $C_{function}\{P(t)\}$. The simplest example is indexing the table by amplitude where $C_{function}(P) = \sqrt{P}$, or indexing by power corresponds to $C_{function}(P) = P$.

Optimum indexing will increase the density of the table in more nonlinear regions, resulting in better predistortion effectiveness. Figure2-2 is the predistorter structure diagram using a LUT.

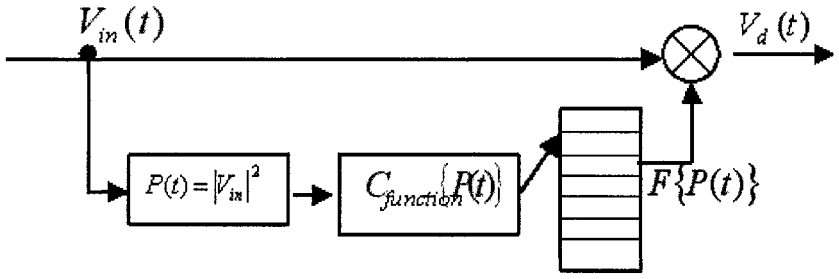

Figure 2- 2 The structure of LUT

$V_{in}(t)$: The complex envelope signal, $V_{in} = \sqrt{I^2 + Q^2} = \sqrt{P}$.

$V_d(t)$: The complex envelope of the predistorted signal.

$F(P)$: The complex gain of the predistorter, which presents AM/AM and AM/PM affects of a PA. The predistorter applies a nonlinearity to produce the predistorted signal $V_d(t)$ according to $V_d(t) = V_{in}(t)F(P)$.

2.4 *Feedback path*

The feedback-processing block includes a dual-channel mixer; which translate the RF input and output signals to the intermediates frequency (IF). A 30MHz IF frequency is chosen in order to cover 45MHz bandwidth. The mixer was designed carefully in order to get the quasi-same complex mixing function in the two paths, which are the bases of

adaptive synthesis. A dual-channel, 12-bits 125MSPS A/D converter is used to digitize the analog input signals of the two mixer outputs.

The two digitized signals are demodulated using a dual-channel digital demodulator in order to extract their digital baseband Q and I components. Dynamic AM/AM and AM/PM characteristics of the amplifier are constructed using the recorded Q and I components of the input and output signals. Based on these nonlinear characteristics of the PA, the LUT entries are directly synthesized using the DSP processor. A connection between the DSP and FPGA, which is used for the implementation of the digital part of the predistorter, was used for uploading the new contents to the LUT. This allows the predistorter to take into account any change in the behavior of the PA that could occur due to temperature drift, aging or biasing point variation. The DSP processor offers a flexible algorithm of updating the LUT. It reads input and output values of the PA. Using these values, the DSP processor execute the algorithm and calculates the new LUT value and writes this value back to the table.

2.5 *Power amplifier*

For the PA, a three-stage HPA for a wireless communication band of 1930-1990 MHz was designed and built for the purpose of this implementation. The first stage is a drive amplifier as gain block. The second stage is built using the LDMOS MRF19045 (Motorola) transistor having output power 9.5Watts average and gain 14.9dB. The third stage uses LDMOS MRF19085 class-AB amplifier with output power 18Watts (42.5dBm) average and gain 13dB. The overall small-signal gain of this lineup is 58dB.

The HPA peak output power at 1-dB gain compression is approximately 49dBm.

2.6 *The DPD system simulation in MATLAB Simulink*

System level simulation provides a solid starting point for building an implementation quickly. The designed components could be integrated into the simulation system to order to assess the overall performance.

Altera DSP builder connects Simulink—from the MathWorks industry leader, system level DSP tool—with Altera industry leading QuartusII development software. It provides a seamless design flow, and allows performing the algorithm in the Matlab software, then performing the system integration using Simulink software. Then, the design is compiled to a HDL file for use in the QuartusII software. It also incorporates Altera intellectual property (IP) cores such as the finite impulse response (FIR) compiler and numerically controlled oscillator (NCO) compiler. We can also optimize the design in Matlab for use in QuartusII software quick timing and simulation comparisons.

By using of the various DSP block libraries and Altera Libraries in DSP Builder, a top-level DPD simulation diagram (figure2-3) is built. The input signal source provides a baseband complex CDMA IS95 signal. The format of the signal is a matrix (2-D array) of discrete sampling data, which comes from a real time signal source after interpolation.

The first part of the diagram is to scale the input signal value as a signed fraction. The calculation is based on fixed-point fraction operation. The LUT is saved in two 2K ROMs as a hex file. The address indexation calculation is based on the signal power ($I^2 + Q^2$). Figure2-4 shows the block diagram of the complex multiplier function.

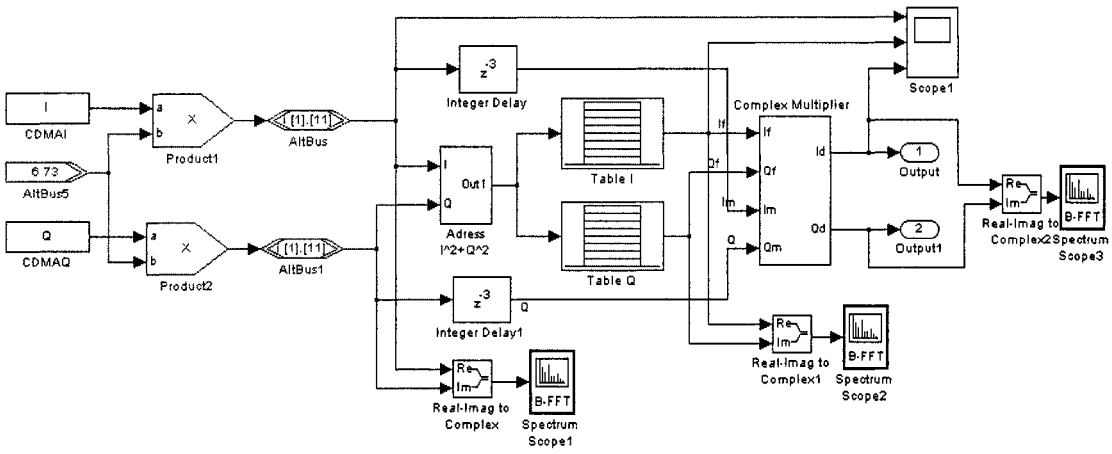

Figure 2- 3 Top simulation block diagram of predistorter in Simulink

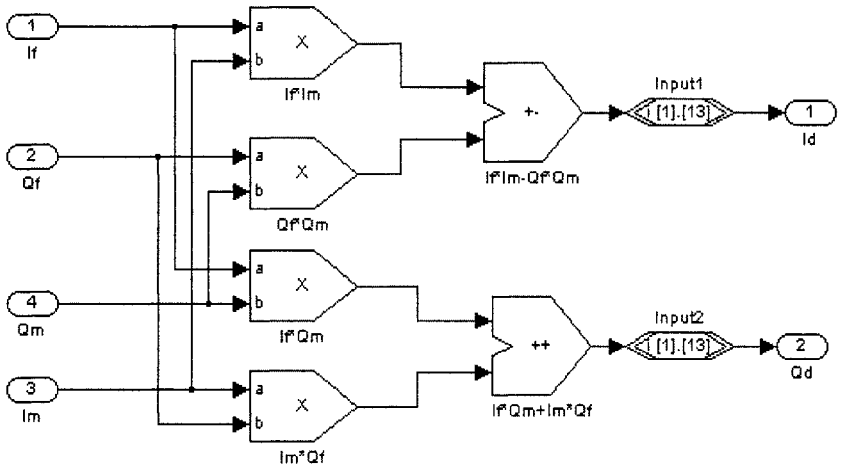

Figure 2- 4 Sub-diagram of complex multiplier

The frequency domain simulation results of the predistorter shown in figure2-5, the spectrum was displayed by the spectrum scope, which computes and displays magnitude-squared FFT of the input signal. The input is a vector with real part-I and

imaginary part-Q. One clearly observes the distorted spectrum from the PA's nonlinear behavior of the PA. The simulation can optimize the parameter such as the data bus width. A 12-bit limited precision can adequately represent the signal quality.

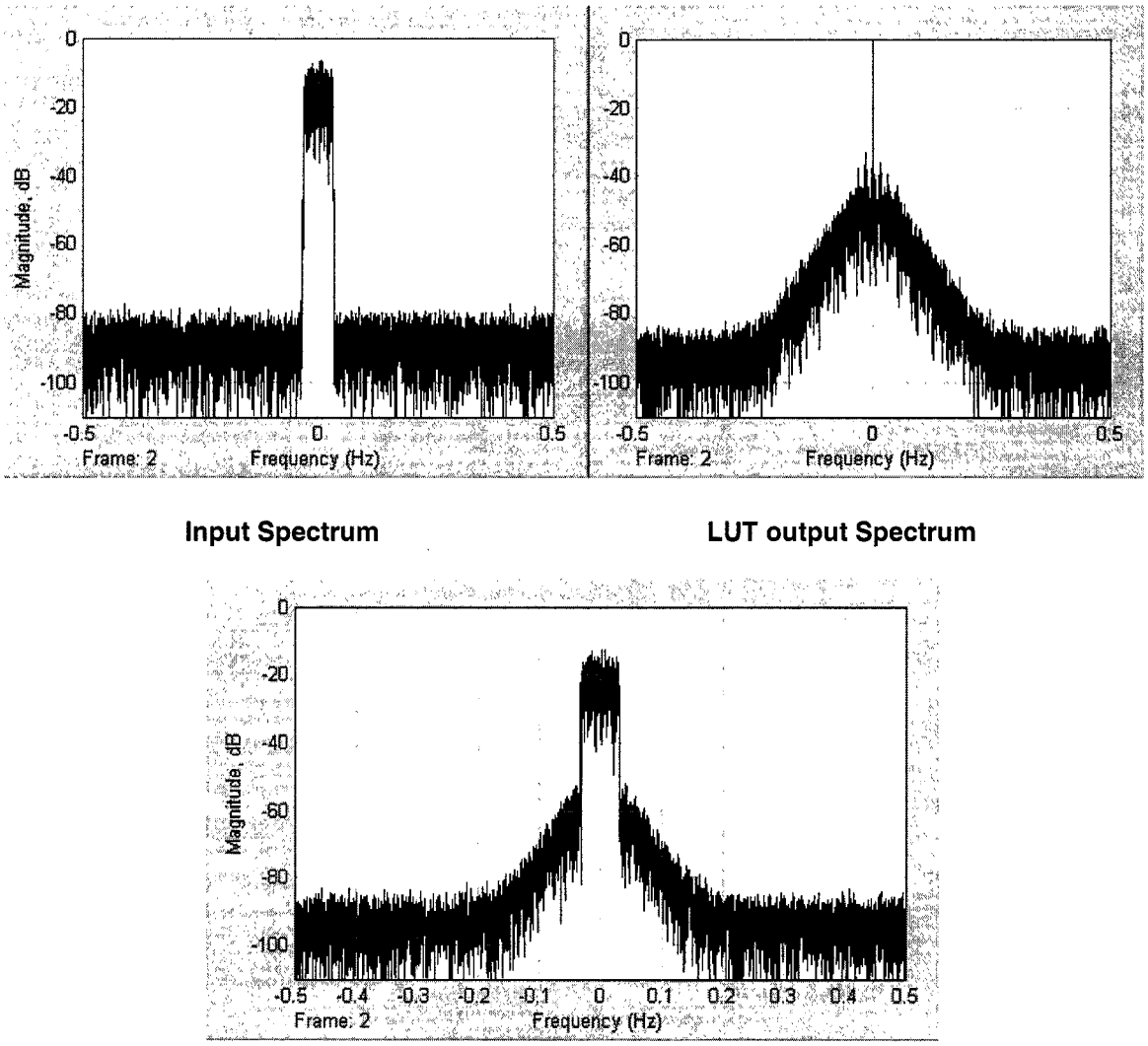

Figure 2- 5 Simulation results in frequency domain

Chapter 3: The Design of Dual Channel Receivers

There are two receivers in the feedback path, which serve for the translation of the RF input and output signals of the PA to intermediates frequencies (IF). The receivers were designed to get the quasi-same complex mixing signals in the two paths. Figure3-1 shows structure diagram of each receiver.

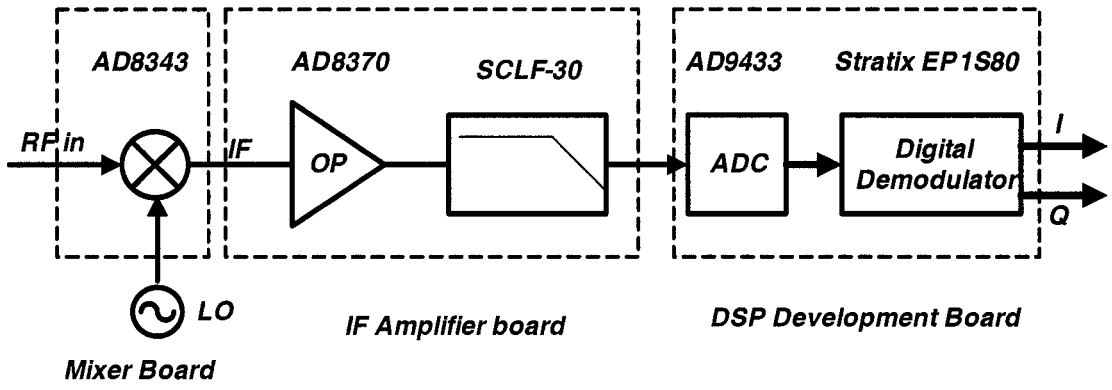

Figure 3- 1 Implementation block diagram of feedback path

The mixer represents a RF to IF down conversion working at 2GHz, which have a wide bandwidth 200MHz on all ports, and a very low intermodulation distortion. An external oscillator at frequency 1.93GHz used as LO is applied to the mixer.

An IF amplifier which follows was also used for adjusting the gain imbalance and DC-offset in the Q and I branches, asides from performing a single-ended to differential signal transformation. The intermediate lowpass filter helps to minimize unwanted high frequency spectra from the mixer, which are aliased down into the first Nyquist zone of

the ADC, and it improves harmonic distortion performance.

After the analog to digital converter, the IF digital signal is demodulated to baseband I/Q, the demodulated signals of two channels (before and behind amplifier) are buffered, which are used for the adaptation analysis.

3.1 The design and implementation of the mixer

3.1.1 Design consideration of the mixer

Recent performance improvements in high-linearity active mixers are making them increasingly attractive to wireless system designers. Compared to the legacy passive mixer, a well-designed high-linearity active mixer offers several advantages, it provides low local oscillator (LO) leakage levels, low LO drive levels, higher output signal levels, and lower solution size (high integration).

Based on the key features and the performances requirements for the mixer, we chose Analog Devices AD8343 (www.analog.com) as main device of the mixer [10]. Having a wide bandwidth on all ports and a very low intermodulation distortion, AD8343 is well suited for demanding receiver channel applications such as W-CDMA [14].

The typical features of AD8343 are listed below:

- Broadband Operation to 2.5GHz
- Conversion Gain: 7.1dB
- Input IP3: 16.5dBm
- LO Drive: –10dBm

- Noise Figure: 14.1dB
- Input P_{1dB}: 2.8dB
- Differential LO, IF and RF Ports

The signal paths are entirely differential and dc-coupled to permit high-performance operation over a board range of frequencies, the AD8343 consists of three parts: BIAS, LO DRIVER, and MIXER CORE (Figure3-1).

Multiplication is the essence of the frequency mixer. The ideal multiplier is expressed in the following trigonometric identity in theory:

$$\sin(w_{sig}t)\sin(w_{LO}t) = 1/2\{\cos(w_{sig}t - w_{LO}t) - \cos(w_{sig}t + w_{LO}t)\} \qquad (3.1)$$

The product of two sine-wave signals of different frequencies is a pair of sine waves at frequencies equal to the sum and difference of two frequencies being multiplied. The down-converted signal is at the frequencies difference of two frequencies being multiplied.

Practical implementations of analog multipliers generally use the LO signal to periodically reverse the polarity of the input signal. In AD8343 mixers, frequency conversion occurs as a result of multiplication of the signal by a square wave at LO frequency. Because a square wave contains odd harmonics in addition to the fundamental, the signal is effectively multiplied by each frequency component of the LO. The output of the mixer will contain signals at: $F_{LO} \pm F_{sig}, 3F_{LO} \pm F_{sig}, 7F_{LO} \pm F_{sig}, 5F_{LO} \pm F_{sig}$.

The signal switching characteristics is illustrated in figure 3-2. The first pane of this figure shows a 1.96GHz sinusoid representing the input signal. The second pane

contains a square wave representing the LO signal at 1.93GHz, which has been hard-limited by the internal LO driver. The third pane shows the time domain representation of the output waveform, and the fourth pane shows the frequency domain representation. The two strongest lines in the spectrum are the sum and difference frequencies arising from multiplication of the signal by the LO fundamental frequency. The weaker spectral lines are the results of the multiplication of the signal by various harmonics of the LO square wave.

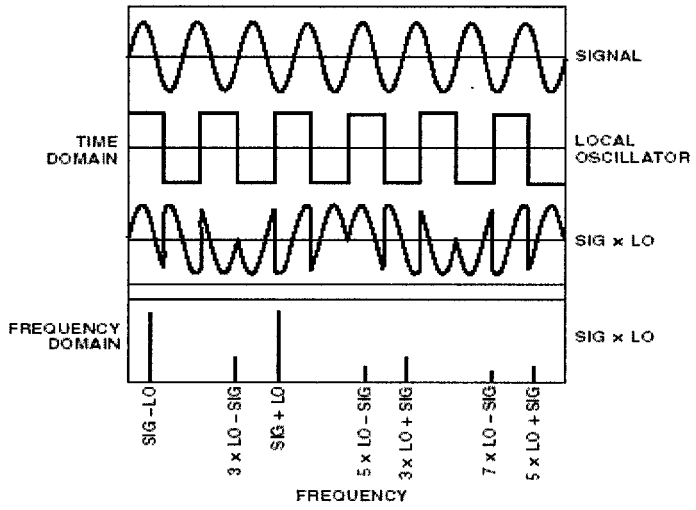

Figure 3- 2 Signal switching characteristics of the mixer

The AC signal connection diagram of the mixer is shown in Figure3-3. The input signal single-ended to differential conversion is obtained through a 1:1 RF balun, and is then reactively matched to the impedance presented by the emitters of the core, a typical input matching network that is designed to match the AD8343's differential input impedance to the differential output impedance of the balun. The matching network also

provides bias currents to these emitters. Similarly, the local oscillator signal at a level of –12dBm to –3dBm is brought in through a 1:1 RF balun undergoes a single-ended to differential transformation, and then it is applied to the 50Ω differential LO port. The differential IF output signal is taken through a 4:1 impedance ratio transformer that reflects a 200Ω differential load to the collectors, this output coupling arrangement is reasonably broadband.

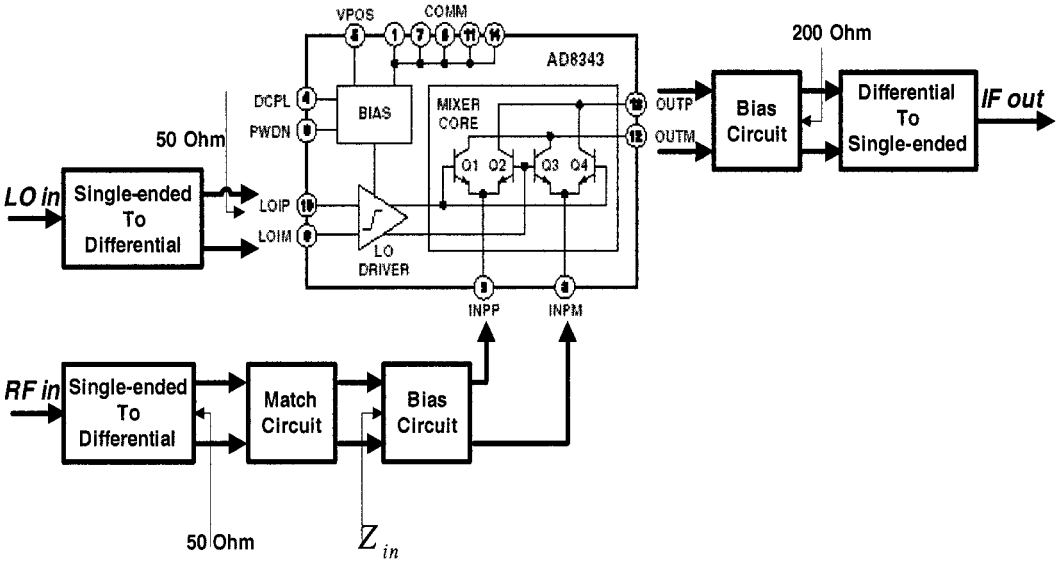

Figure 3- 3 The basic AC signal connection diagram of the mixer

3.1.2 Single-ended to differential conversion

The RF input of mixer is single-ended, due to the AD8343 is designed to accept differential input signals for the best intermodulation performance, a conversion balun is needed to produce the required balanced waveforms and impedance match. The balanced circuit topologies provide the near-perfect, repeatable symmetry of the integrated circuit

(IC) layout, and results in low LO leakage.

The balun LDB211G9005C-001 from Murata (www.murata.com) is a high-performance RF impedance converter, which is used in both RF input port and LO port. The main features of input RF Balun are:

- Ratio of input and output impedance: 1:1
- Frequency range of input: 1.9GHz-2.0GHz
- Insertion loss in-band: < 1dB

3.1.3 Input matching considerations

The input is a RF signals operating around 1.92GHz-2.0GHz, a suitable impedance match network is necessary. The design of the input match circuit should be undertaken with two goals in mind: matching the source impedance to the input impedance of the AD8343, and providing a dc bias current path for the bias setting resistors.

The maximum power transfer into the device will occur when there is a conjugate impedance match between the signal source and the input of the AD8343. This match can be achieved with the differential equivalent of the classic "L" network, as illustrated in Figure3-4. The figure gives two examples of the transformation from a single-ended "L" network to its differential counterpart.

To design an accurate matching network, we have to make a differential impedance measurement at the board location where the matching network will be installed. When the frequency is in excess of 500MHz, the particular board traces and

pads transform the input impedance.

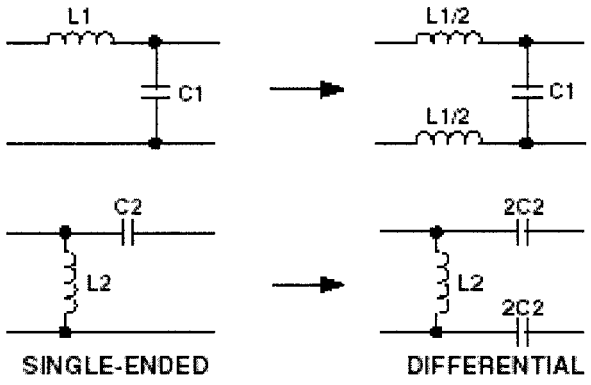

Figure 3- 4 Single-Ended-to-Differential transformations

1. Establish Target Impedance: The input impedance of the matching network, loaded with the AD8343 input impedance (including ballast resistors), should be the conjugate of the output impedance of the single-ended to differential network (input balun), which is 50Ω.

2. Input matching network consists of four lump reactive components, the schematic of matching circuit is shown in figure3-5. The target impedance 50Ω is established, the next step in matching to the AD8343 is to measure the differential impedance at the location of the first matching component Z4.

Doing the board measurements, one uses a standard two-port vector network analyzer (VNA). After the calibration (1.5GHz to 2.0GHz), connect vector network analyzer ports one and two to the differential inputs of the AD8343.

Before measurements, it is necessary to temporarily install jumpers at the

component position of Z1 and Z3, assuming Z4 is the desired component location, and disconnecting the input balun. And then extend the reference plane to the location of first matching component. This is accomplished by solidly shorting both pads at the component location to GND (Power to the board must be off) adjust the VNA reference plane extensions to make the entire trace collapse to a point at the zero impedance point of the Smith Chart [2].

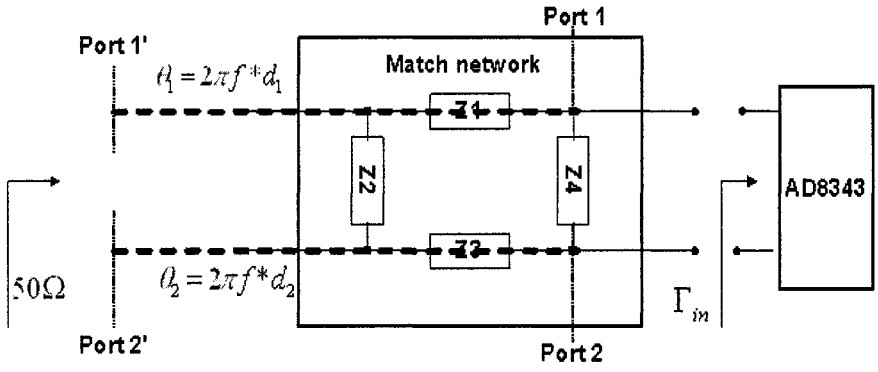

Figure 3- 5 Input matching circuits

$$\begin{bmatrix} S_{11} S_{12} \\ S_{21} S_{22} \end{bmatrix} = \begin{bmatrix} S'_{11}\, e^{j2\theta_1} S'_{12}\, e^{j(\theta_1+\theta_2)} \\ S'_{21}\, e^{j(\theta_1+\theta_2)} S'_{22}\, e^{j2\theta_2} \end{bmatrix} \tag{3.2}$$

Tested the delay value in location Z4 is: $d_1 = 261ps$ at S_{11}, $d_2 = 263ps$ at S_{22}

Then, $\theta_1 = wt_1 = 2\,f\pi d_1 = 3.21$, $\theta_2 = wt_2 = 2\pi f d_2 = 3.237$

Where the factor $e^{\pm j\theta}$ accounts for the phase difference of the waves at the different reference planes.

After removing the short, apply power to the board, and take readings of S parameters of port1', port2', then use the (3.2) convert S parameters of port1', port2' to port1, port2. Finally we use Konstroffer's formula (3.3) to convert the two-port parameters to one-port differential Γ_{in} [28].

$$\Gamma_{in} = \frac{(2S_{11} - S_{21})(1 - S_{22} - S_{12}) + (1 - S_{11} - S_{21})(1 + S_{22} - 2S_{12})}{(2 - S_{21})(1 - S_{22} - S_{12}) + (1 - S_{11} - S_{21})(1 + S_{22})} \tag{3.3}$$

Figure3-6 shows S parameter measurement results. The left figure is the two-port S parameters at reference plane 1' and 2'; the right figure is the one-port differential S parameters Γ_{in} at reference plane 1 and 2.

We got $\Gamma_{in} = 0.818\angle -13$ at frequency 1.96GHz, which represents the source reflection coefficient of matching network

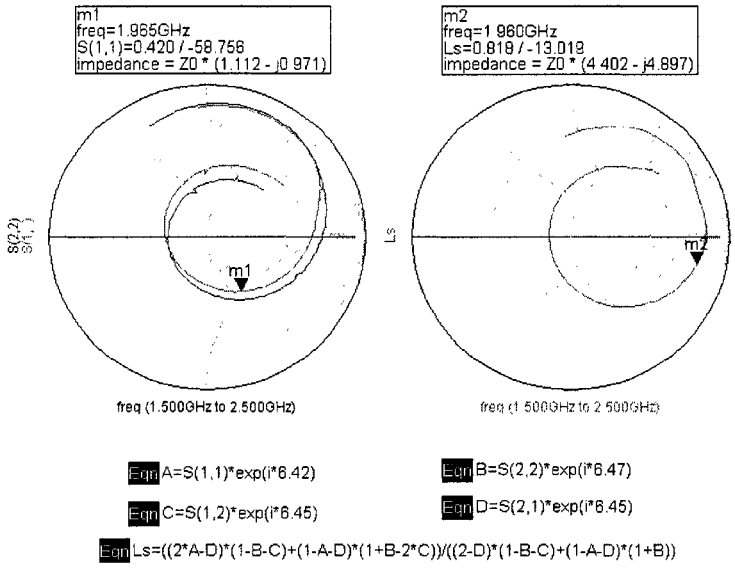

Figure 3- 6 S parameters and Γ_{in} of differential input

3. We perform the design of a matching network utilizing standard impedance matching techniques. The network may be designed using single-ended network values, and then converted to differential form.

Figure3-7 shows a theoretical design of a series C/shunt L network applied between 50Ω and the load at 1.96GHz. The theoretical value of first shunt capacitor is $C_{shunt} = 0.305pF$ for the initial matching component Z4 (from point 1 to point 2 in Smith Chart), this value is not available, so $C_{shunt} = 0.36pF$ is placed in the first shunt matching location Z4.

For the calculation of second components Z1 and Z3, the reference plane is extended to the location of the series matching components. The calculation of series inductor value required moving from the point 2 to point 3 (figure3-7), we got $L_{series} = 12.1nH$.

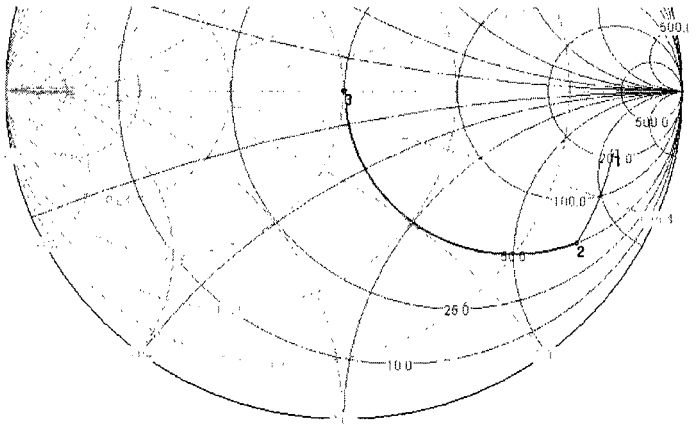

Figure 3- 7 Theoretical design of the input matching circuit

Finally, a single-ended of "L" network is transformed to its differential

counterpart according to figure3-4, the values are: $C_{shunt} = 0.36pF$, $L_{series} = 6.0nH$.

3.1.4 Output interface

The output interface works at low frequencies (central frequency 30MHz and bandwidth 45MHZ); the AD8343 requires a differential load in order to achieve optimal devices performance, and a differential load will provide the best LO to output isolation and best input to output isolation. The output interface circuit has three considerations:

- The output impedance match (AD8343 at low frequencies is 200Ω).
- The output of AD8343 comprises balanced pair open-collector outputs, these should be biased to about same voltage as is connected to VPOS (+5V).
- Differential to single-ended conversion.
- Operation frequency from 2MHz to 60MHz.

The mixer requires a single-ended IF output. The transformer is used to perform the differential to single-ended conversion. Internal IF amplifiers that perform the differential to single-ended conversion are available in some low-power active mixers but perform poorly in high-linearity applications unless the mixer's output is filtered before IF amplification.

Transformer TC4-1T from Mini-circuit (www.minicircuits.com) is used for output interface; it is a surface mount component with insertion less than 1dB in band 1.5MHz-100MHz. The primary winding of the transformer is center tapped. Apply VPOS to the tap, so that collector dc bias voltage should be equal to the supply voltage (figure3-8). The transmission ratio of transformer is 4:1 to obtain desired output impedance 50Ω . All

the AC coupling capacity must bigger than 4.7uF to keep flatness of output frequency response at lower frequency side.

A lowpass filter is used to reject unwanted high frequency spectra from RF, LO leakage and frequency conversion of multiplication by a square wave at LO frequency, to order to improve harmonic distortion performance before going to IF amplifier. The filter is built to filter out high frequency components $F_{LO}, 5F_{LO} \pm F_{sig}, 3F_{LO} \pm F_{sig}$. A RF lowpass filter LFL21902MTC1A018 from Murata is chosen. The lowpass filter has cutoff frequency 1.5GHz, in-band insertion loss of less than 0.1dB. The attenuation ratio is larger than 40dB at out-of-band.

3.2 The implementation of the mixer

The implementation of the mixer includes two parts: one is single channel board; it is configured for ease in making device impedance measurements as part of the process of developing suitable matching networks for a final implementation. The second is a dual channel board, which designed for operating the AD8343 in a single-ended environment and includes two channels at both the input and output of the PA. The schematic of a single channel mixer is shown in Figure3-8

The critical part of the mixer PCB layout:

A) Selection of substrate and width calculation of 50Ω micro-strip in ADS

The selection criterion of substrate bases on the reasonable micro-strip width coincide with the operation frequency and pad size of AD8343 package, the chosen substrate is RO3006 (www.rogers-crop.com), the main parameter is: H = 25mil, Hu =

500mil, $\varepsilon_r = 6.15$, T = 0.68mil, $u_r = 1$, TanD = 0.0025, Cond = 5.6e+7, Rough = 0. The 50Ω trace width is W = 35.9mil at frequency 1.96GHz.

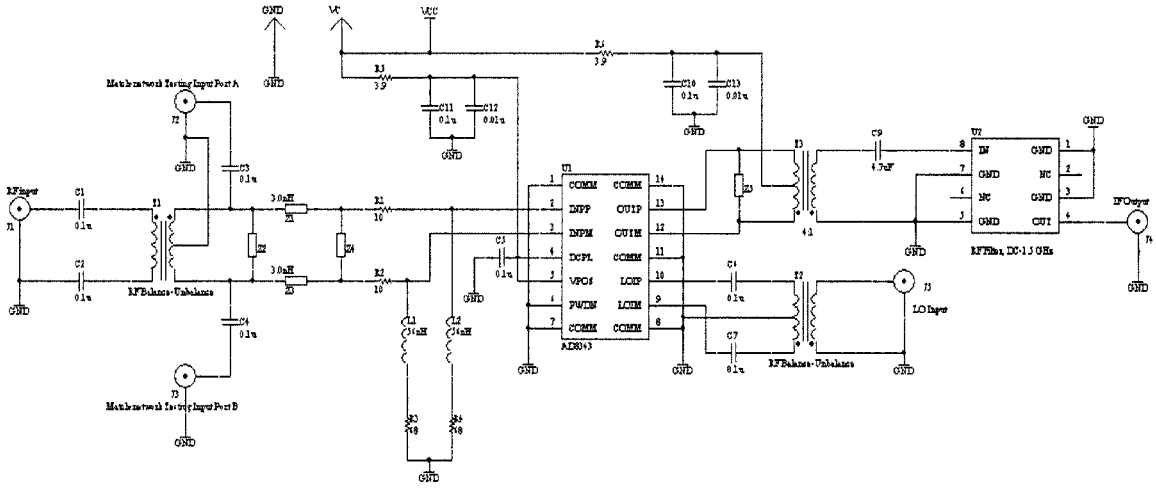

Figure 3- 8 The schematic of one channel mixer board

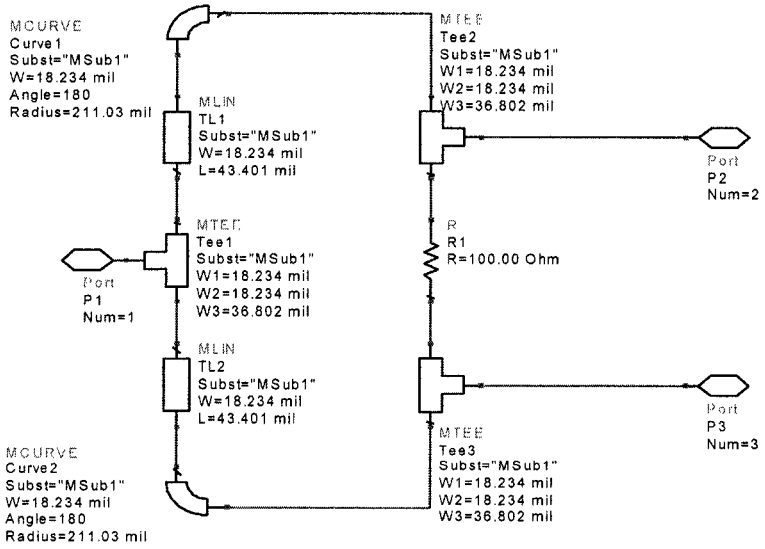

Figure 3- 9 Wilkinson coupler dimension optimization in ADS

B) The design of LO input power divider for dual-channel mixer

The power divider used in the LO input is a 3-dB Wilkinson coupler [2]. It is a three-port network that divides equally the input power at port1 and between port2 and port3. The signals at port2 and port3 are of equal amplitude and phase. The design of Wilkinson divider is shown figure3-9. The power divider works at 1.93GHz. If the input power level is –5dBm at the port1, the output power level is –8dBm at port2 and port3.

C) PCB layout of dual-channel mixer

The PCB layout is designed using ProtelXP software. The critical rules for the lay out of the mixer board using the AD8343 device are:

- Keep RF signal lines as short as possible to minimize losses and radiation.
- Always use controlled-impedance lines on all high-frequency input and output, use low-inductance connections to ground on all GND pins.
- At all differential ports keep the differential lines together and keep of the same length to ensure signal balance.
- The PCB layout should provide a large ground pad under the device for proper RF grounding and thermal performance.
- To minimize inductance, route the ground pins of the device to the large ground pad by using multiple vias.

The PCB layout of the dual-channel mixer is shown in figure3-10. Figure3-11 is the photograph of dual-channel mixer board, the LO port of two channel is located in the middle of the board, the LO signal passes through a Wilkinson divider that divides equally the input power to LO input of each channel.

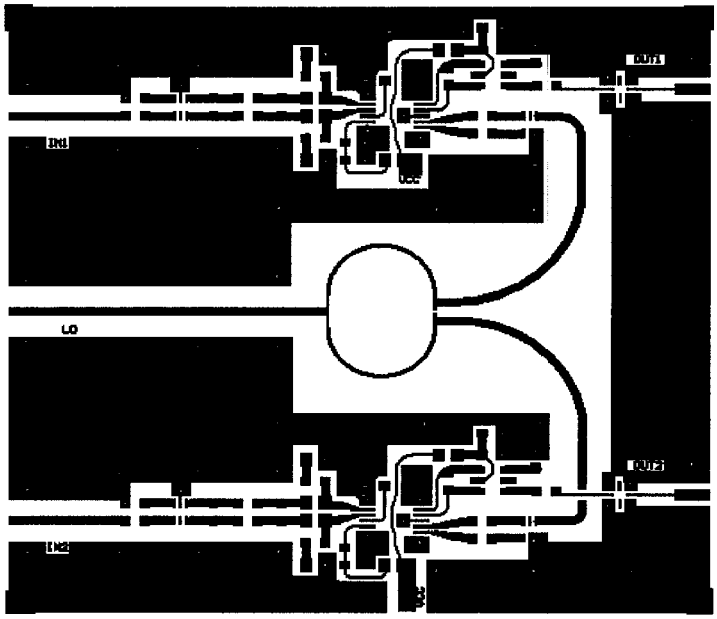

Figure 3- 10 PCB layout diagram of dual-channel mixer board

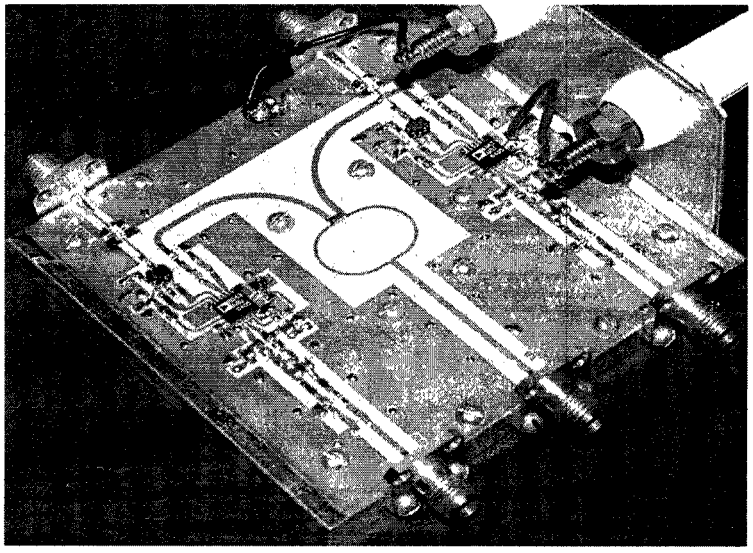

Figure 3- 11 Photograph of the dual channel mixer

3.3 Measurement results and analysis

The measurement of the mixer is based on a one-channel mixer. The testing configuration is showed in figure3-12. We use a SMIQ 03B Vector Signal Generator in combination with an in-phase/quadrature (I/Q) modulation generator (AMIQ) as a RF source, which creates a modulated signal with carrier frequency 1.96GHz. Signal Generator 2031 as the LO source, which provides a 1.93GHz sine wave. The spectrum analyzer 8563A is used to display the output.

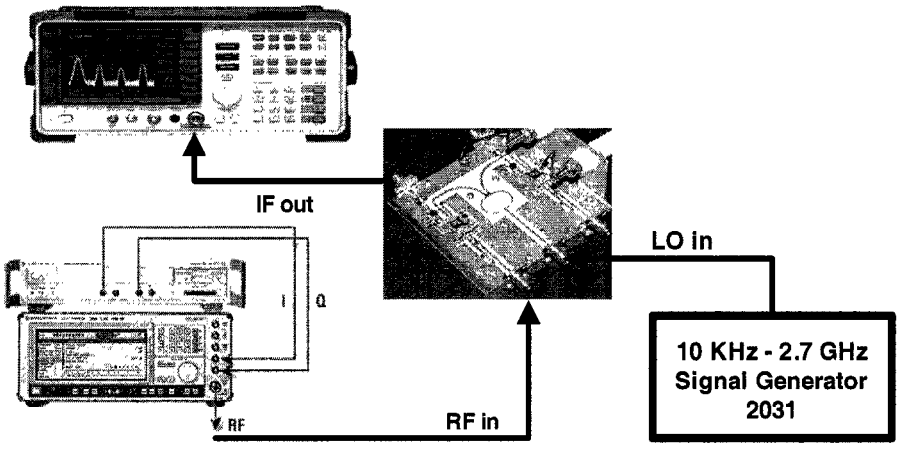

Figure 3- 12 The block diagram of the mixer testing

Measurement results are summarized below:

1. Output frequency characteristics

Figure3-13 shows the down conversion frequency characteristic. The input RF power level is –12dBm, frequency varies from 1.93GHz to 2GHz. The LO input power level is –5dBm and the frequency 1.93GHz. From the chart, the mixer presents a

conversion gain of 5.5dB (figure3-13), and less than 0.5dB gain variation in frequency range 1.93GHz to 1.99GHz.

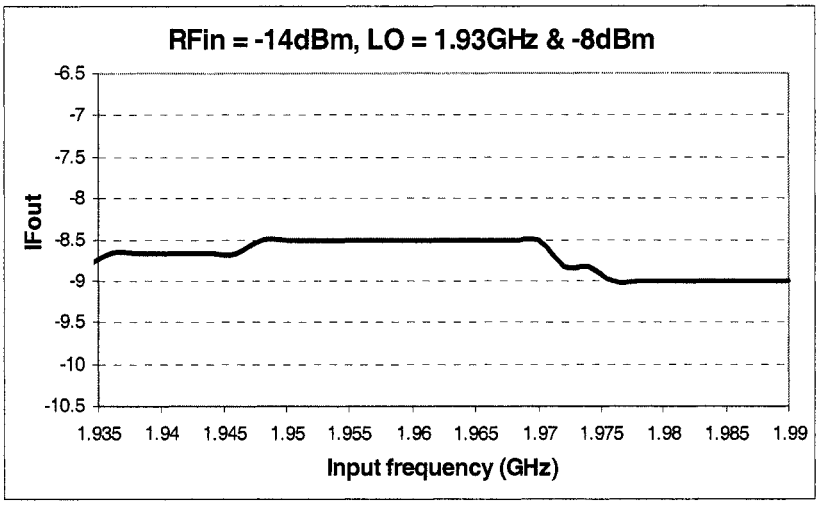

Figure 3- 13 Frequency performance of down-conversion

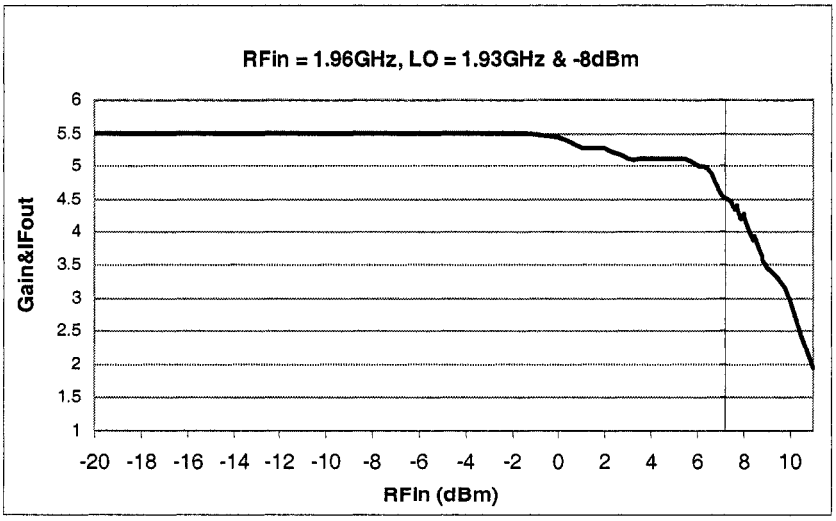

Figure 3- 14 Input P_{1dB} compression point

2. Input P_{1dB} compression point

Figure3-14 shows the measured gain performance over the input power level range (varying from –20dB to +12dBm). The input frequency is 1.96GHz, the LO power level is –5dBm at 1.93GHz. From the chart, we get an input P_{1dB} compression point at 7.4dBm, thus the mixer shows a better linear performance. The reason for the improvement in linearity is due to the sacrifice of conversion gain.

3. Two-tone test and intermodulation distortion performance IP3

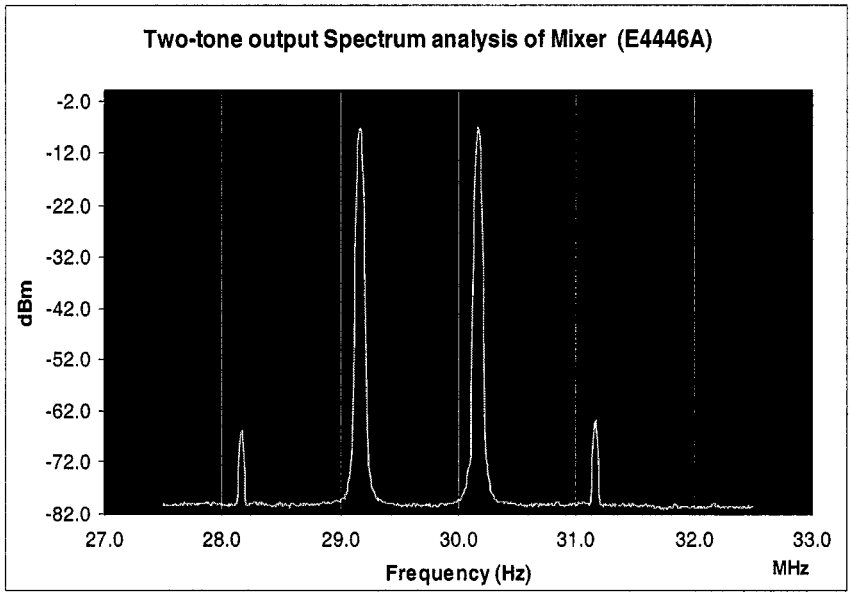

Figure 3- 15 The nonlinear output spectrum of the mixer with tow-tone signal

Using a two-tone signal, we can see more precisely nonlinear characteristic. The power level of the two-tone is –12dBm with two excitations of equal amplitude and

1MHz space (f1 = 1959.2MHz, f2 = 1960.2MHz), IF output level is P_{lin} = -7.1dBm at frequency 30.2MHz.

Figure3-15 shows the output spectrum driving with two-tone signal, the 3rd intermodulation distortion level IM3 = -64dBm at frequency 31.2MHz, we get 56.9dBc intermodulation performance.

Using the equation: $IM_3 = 3P_{lin} - 2IP_3$ we got output IP_3 = 21.4dBm. If the conversion gain G = 5.5, then the input IP_3 = 21.4 – 5.5 = 15.9dBm.

4. Testing with a multi-carrier W-CDMA signal

The RF input is a W-CDMA signal (101) with wider bandwidth (15MHz) with two carriers and central frequency at 1.96GHz, the spectrum of "101" stands for three-carrier W-CDMA signals. The LO input signal is at frequency of 1.90GHz & power level of –5dBm. The Central frequency of IF output locates at frequency 60MHz.

Figure3-16 shows the measurement results, the measurement traces were captured using a PSA/ESA Spectrum Analyzer (E4446A). The ACPR value of input signal is 57dB, and the output ACPR value of the mixer is around 56dB.

The mixer presents superior down conversion performance over 60MHz a bandwidth, and handles multi-carrier W-CDMA signal without obvious intermodulation distortion.

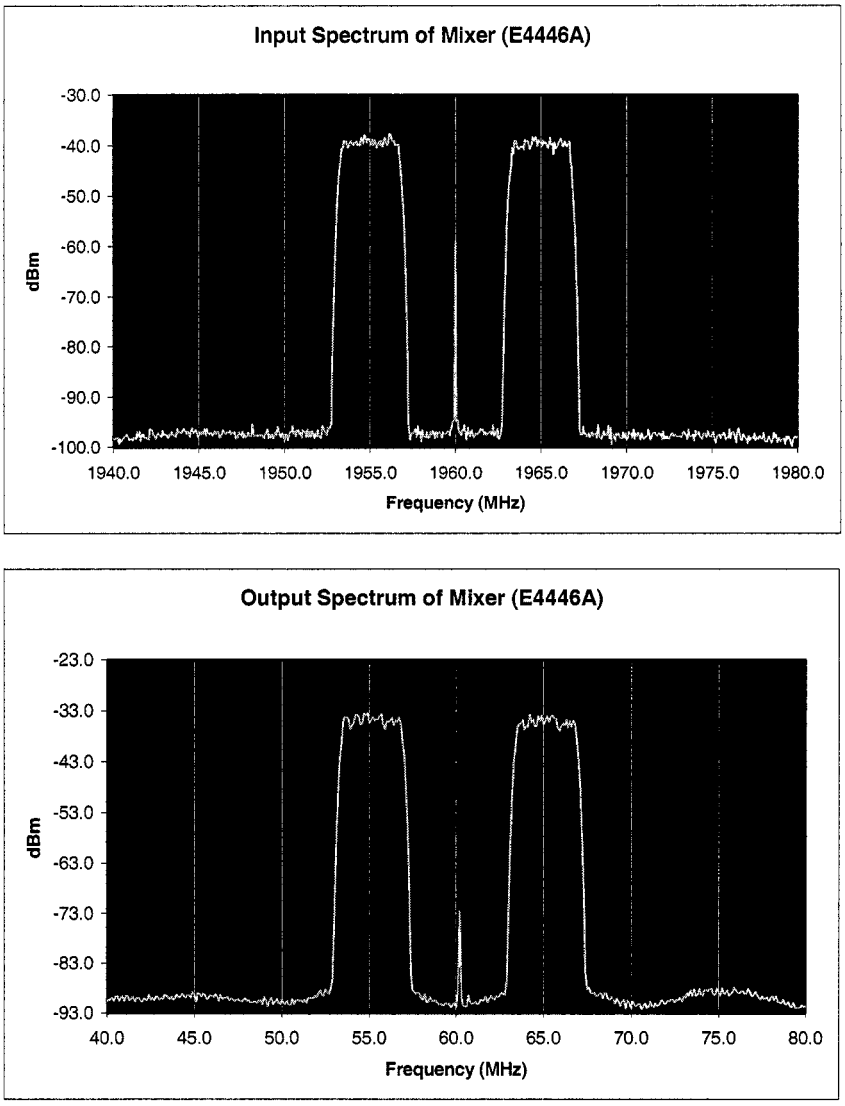

Figure 3- 16 The mixer output spectrum with multi-carrier W-CDMA signal

3.4 Design of the digitally variable gain IF amplifier

The IF amplifier is a conditioned driver between the mixer and the A/D converter. It provides adjustable gain monitored using the parallel port of the PC using the ADI-

Evolution software, and a high output level. The input and output requirements of IF amplifier is listed below:

- Broadband operation to 60MHz,
- Input: voltage level –6dBm & 50Ω , AC coupling, single-ended,
- Output: average voltage level +7dBm & 50Ω (1V peak-to-peak), AC coupling, single-ended,
- Gain: 16dB variable, insertion loss inband: ±0.5dB.

The main device used in IF amplifier is AD8370 from ADI. AD8370 is a digitally controlled variable gain amplifier. It provides precision high gain, high IP3, low noise figure and wide bandwidth. The features of AD8370 [15] are listed below:

- Programmable gain range using serial 8-bit digital interface control

  Low range: -11dB to +17dB, High range: +6dB to +34dB
- Differential impedance: 200Ω differential input, 100Ω differential output
- Two-tone IP3: +35dBm & 70MHz, -3dB bandwidth: 750MHz

We configured the AD8370 low gain mode, a vernier 7-bit transconductance (Gm) stage provides 22dB of gain range at better than 1dB resolution. Gain control of AD8370 is through a serial 8-bit gain control word. The MSB selects between the two gain ranges: low gain –11dB to 17dB, or high gain +6dB to +34dB, and the remaining 7 bits adjust the overall gain in precise linear gain steps. There are 128 possible gain codes (2^7). The theoretical linear voltage gain can be expressed with respect to the gain code as:

$$A_v = GainCode * Vernier * (1 + (\Pr eGain - 1) * MSB) \qquad (3.4)$$

A_v : The linear voltage gain. MSB = 1 high gain or MSB = 0 low gain

The GainCode: The digital gain control word minus the MSB (final 7-bit)

Vernier = 0.055744 V/V, PreGain = 7.079458 V/V

With the desired frequency range 1.5MHz to 60MHz, AC coupling capacitors C_{AC} should be used to block any potential dc offsets present at the AD8370 input and output, and present zero impedance inband, a value 4.7uF is chosen to order to keep flatness of frequency response.

At the output, AD8370 drives a lowpass filter with 50Ω single-ended load, and we use a transformer TC2-1T from Mini-circuits as an impedance matching device and a differential to single-ended converter. At the input side, transformer TC4-1T is used for the input interface to the mixer, and it works as impedance matching and single-ended to differential conversion. Figure3-17 is the IF amplifier block diagram.

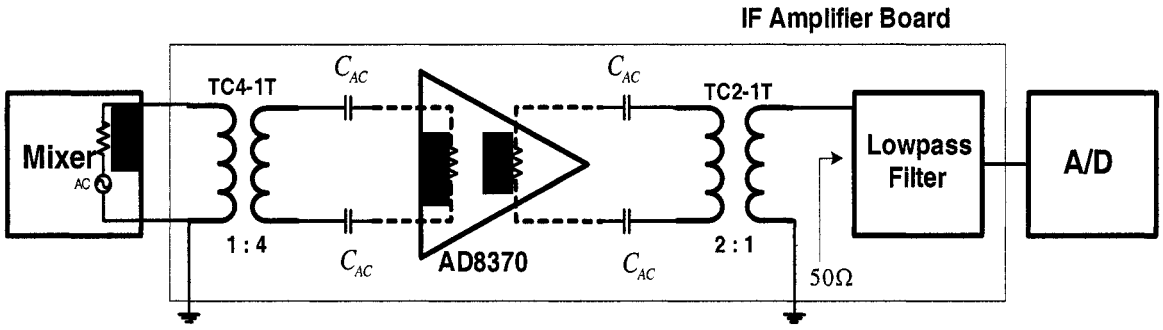

Figure 3- 17 Interface block diagram of IFamplifier

The intermediate lowpass filter used to minimize unwanted high frequency spectra from being aliased down into the first Nyquist zone of the ADC, and to improve the

harmonic distortion performance. We consider the type of filter according to the high frequency rejection required for the ADC interface, frequency response flatness and group delay in pass-band 1.5MHz-60MHz. The device SCLF-65 from Mini-Circuits was chosen, and the specifications are:

- Pass band DC–65MHz, 3dB point at 71MHz
- Inband loss < 0.5dB, Stop band loss > 40dB
- Inband group delay <10ns

The schematic and PCB layout diagram of the IF amplifier board is shown in figure3-18 and figure3-19. The board is used with the AD8370 control software that allows serial gain control from most computers. By adjusting the slider bar in the control software, the gain code is automatically updated to the AD8370.

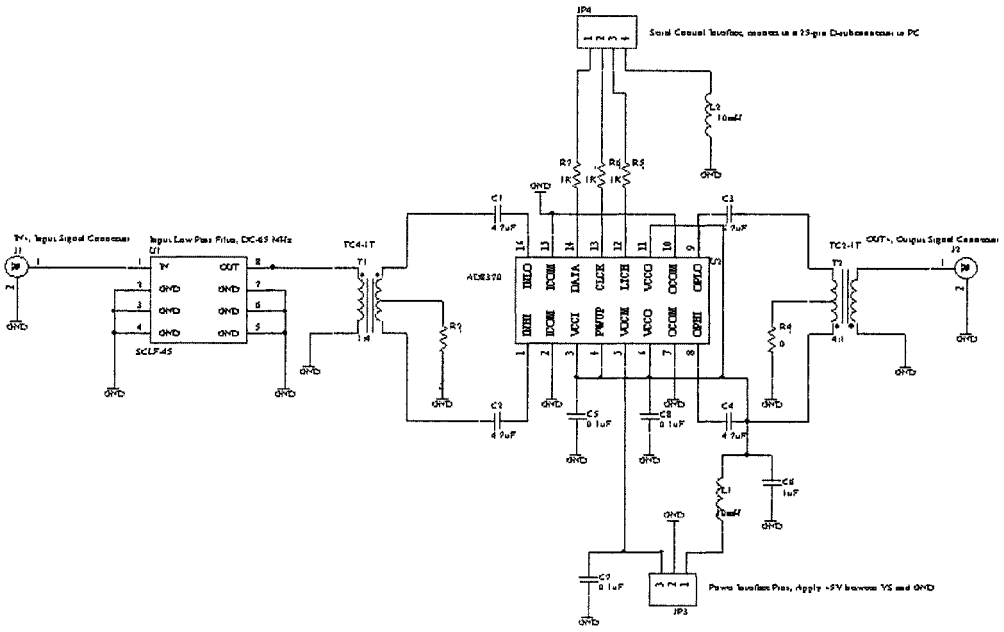

Figure 3- 18 The schematic of the IF amplifier

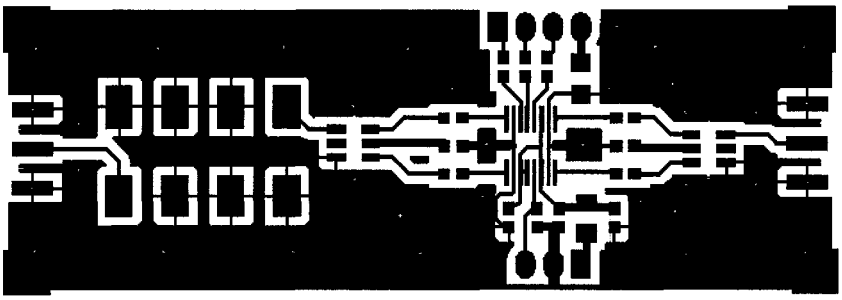

Figure 3- 19 PCB layout of the IF amplifier

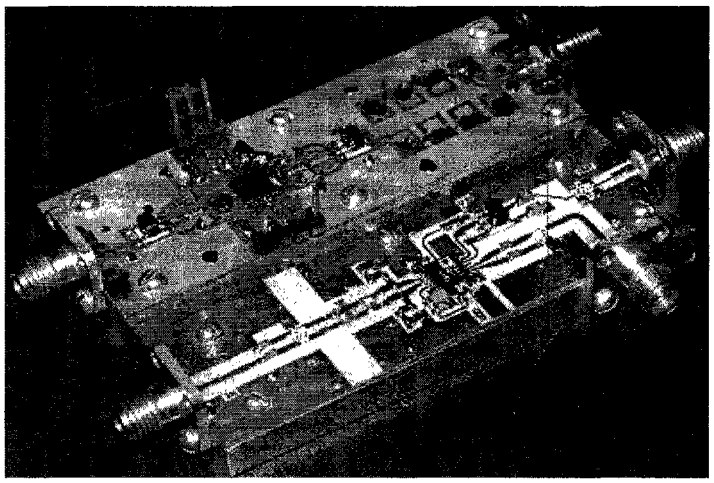

Figure 3- 20 Photograph of the one-channel mixer + IF amplifier

3.5 Measurement results and analysis of the receiver

The measurement is made based on the one channel receiver (Mixer + IF Amplifier). We used the same measurement configuration (figure3-12). The output of the mixer is connected to the input of the IF Amplifier. JP4 (figure3-18) in the IF Amplifier board is connected via a cable to the parallel port of the computer. By adjusting the slide

bra in the control software, the IF amplifier outputs a voltage level of +7dBm for a single frequency point, the IF amplifier obtains a gain around 15dB.

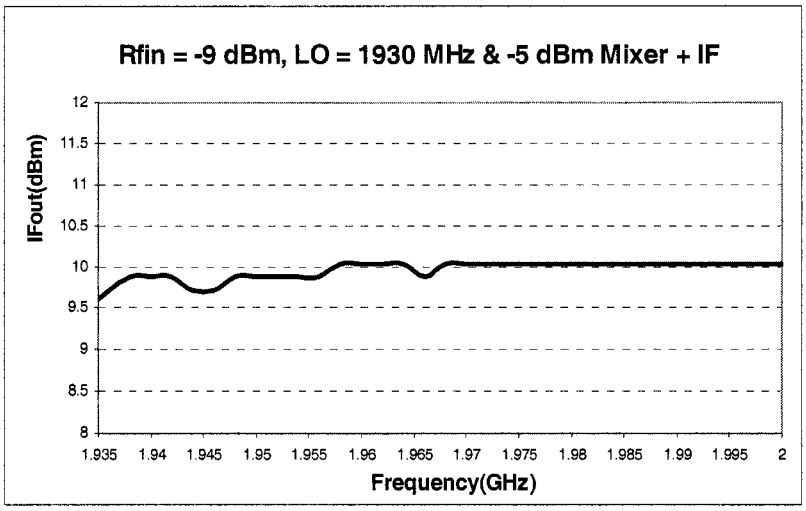

Figure 3- 21 Frequency characteristic of the receiver

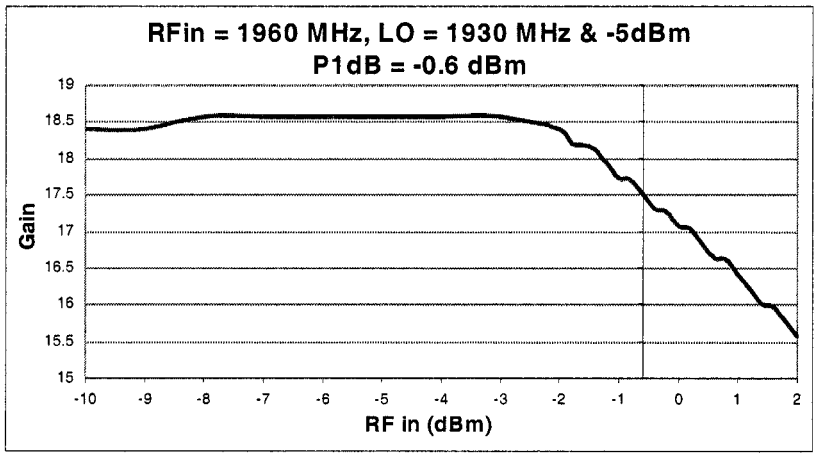

Figure 3- 22 Gain performance and Input P_{1dB} of the receiver

Several measurements were made. The following (figure3-21, figure3-22) present the typical performance results of the one channel receiver. It shows that the receiver presents less than a 0.5dB gain variation in the output frequency range of 1.5MHz-60MHz, and a total 19dB system gain.

Using two-tone signal, the input voltage level is –12dBm with the two excitations of equal amplitude and 1MHz spacing at central frequency 1.96GHz. By adjusting the slide bar, IF amplifier outputs a voltage level of P_{lin} = +7dBm at a frequency of 30.2MHz.

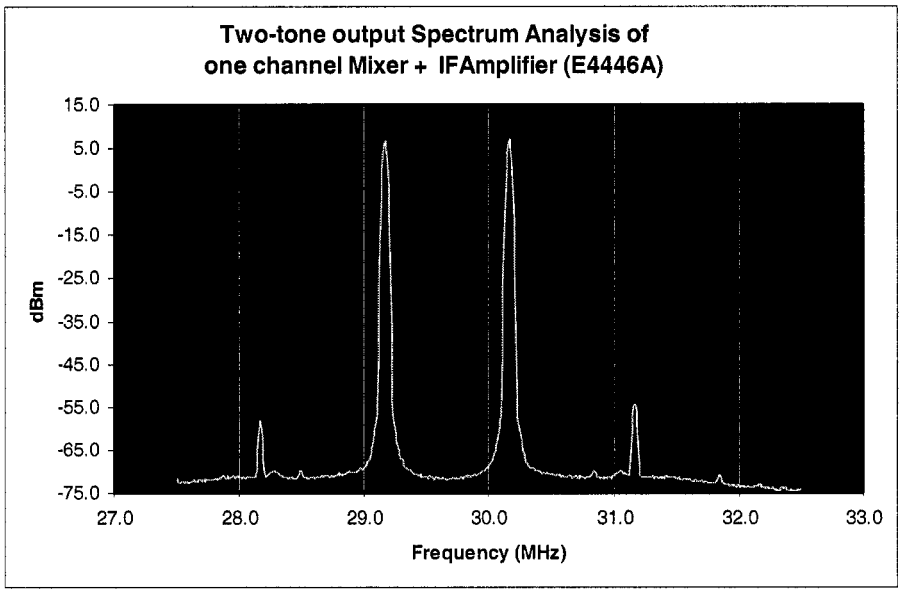

Figure 3- 23 Intermodulation performance of the receiver with the two- tone

Figure3-23 is the output spectrum driving with the two-tone signal, the 3rd intermodulation distortion level IM3 = -54.3dBm at 31.2MHz, we obtain 61.3dBc intermodulation performance.

With the equation: $IM_3 = 3P_{lin} - 2IP_3$ output $IP_3 = 37.6$dBm.

Total gain: G = 19, input $IP_3 = 37.6\text{-}19 = 18.6$dBm.

Comparing the measurement results Mixer + IF with the mixer only. The IF amplifier achieves reasonable gain and low intermodulation distortion. It is capable of driving the ADC with output voltage level +7dBm (1V peak-to-peak).

Chapter 4: The Design of Digital Demodulator and Digital Predistorter Using the Altera FPGA

4.1 Implementation environment of DDEM and DPD

The DPD and DDEM are designed as well as implemented using Altera DSP hardware environment (DSP Development Kit). Altera DSP Development Kit includes the Stratix DSP development board, DSP Builder, the QuartusII development software, MATLAB/Simulink evaluation and simulation software. QuartusII software provides a complete software environment for implementing a hardware circuit design. It supports multi-level FPGA system design, synthesis, place-and-route, verification, and device programming. The Altera Stratix DSP development Board is a hardware verification environment, which enables debugging and verifying both functionality and timing of design [16] [17].

The board includes the following components and interfaces:

- Stratix device EPS1S80B956C6
- Two12-bit 125MHz Analog-to-Digital Converters A/D1 and A/D2 (AD9433, Analog Device) [20] [21].
- Two14-bit 165MHz Digital-to-Analogy Converters D/A1 and D/A2 (DAC904, Texas Instruments).
- Memory subsystem: 2Mbytes of SRAM and 64Mbits of flash memory.
- Configuration options: ByteBlaster II downloads cables.

- Debugging interface.

Expansion interface: Adapter1 for ADI daughter card AD9430, Adapter2 for DSP processor interface.

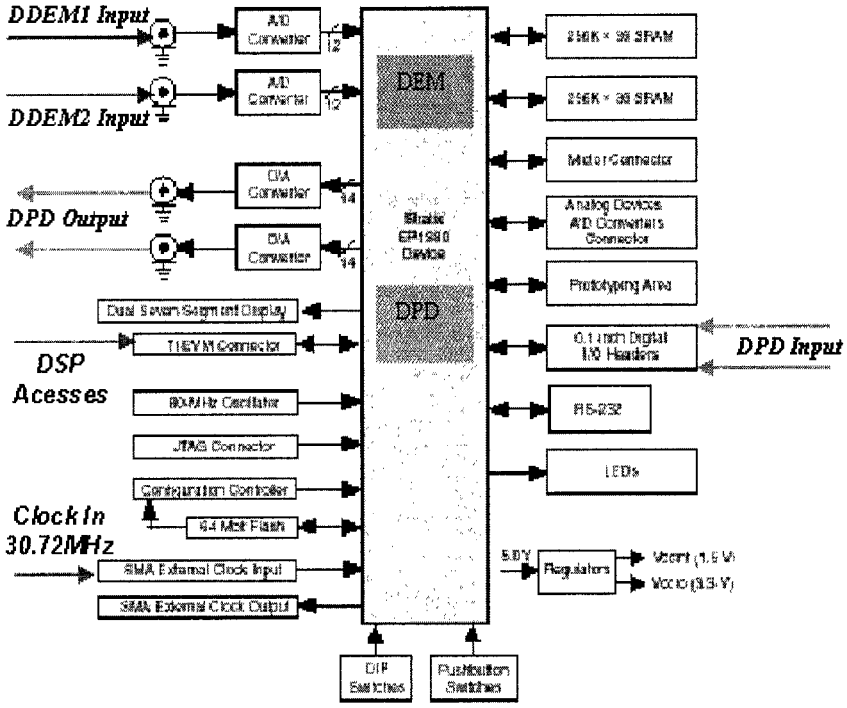

Figure 4- 1 Stratix EP1S80 development board interface diagram

Figure4-1 acknowledges interfaces- DDEM1/DDEM2 Input and DPD Input/Output in the design. The interface and system configuration of the DDEM and DPD are discussed below:

4.1.1 Interfaces and configuration of DDEM and DPD in DSP board

1. Two Analog Input A/D1 and A/D2 are utilized as input ports for dual-channel IF

digital demodulator DDEM.

- The analog IF input is wideband, AC-coupled, which is configured as signal-ended with 50Ω impedance
- The analog input voltage range is $1V_{p-p}$
- Two 12-bit A/D converters produce samples at rate of 122.88MSPs
- The output data format of A/D converter is fraction two's complement

2. Digital I/O Interface -- Baseband digital input port, Analog Output D/A1 and D/A2 as analog baseband output ports.

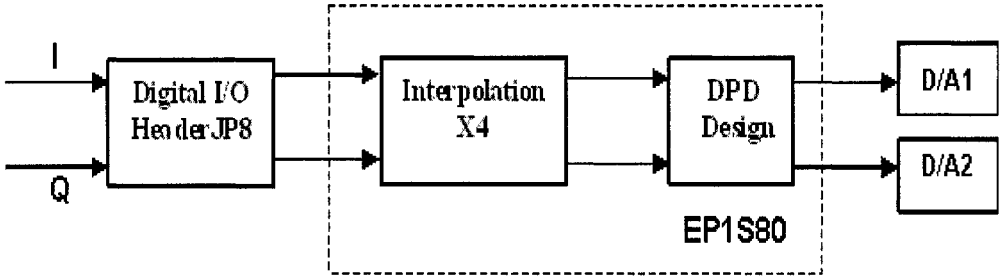

Figure 4- 2 The functional block diagram of the DPD in the DSP board

- Digital I/O header JP8 (DSP development board) is used for digital baseband input ports, which is connected directly to Stratix device.
- The baseband digital signal has format of 14bits, unsigned with a sampling rate of 30.72MSPs.
- The data output of the DPD design is fraction two's complement format. The sampling rate is 122.88MHz after interpolation (4 times input sampling rate).
- Two D/As receive 14-bit sampling data at a rate of 122.88MSPs and expects data in

an unsigned binary format.

- The analog output from each D/A is single-ended, DC-coupled, and the output voltage range is $1V_{p-p}$.

4.1.2 System clocks and distribution

The Stratix EP1S80 DSP development board can obtain the clock source from the on-board 80MHz crystal oscillator or from an external clock. The board provides independent clocks from enhanced, fast PLL to the A/Ds, D/As and other components that required stable clock sources. As the application requirement we use the external slave clock input (JP1), which is synchronized with input sampling data.

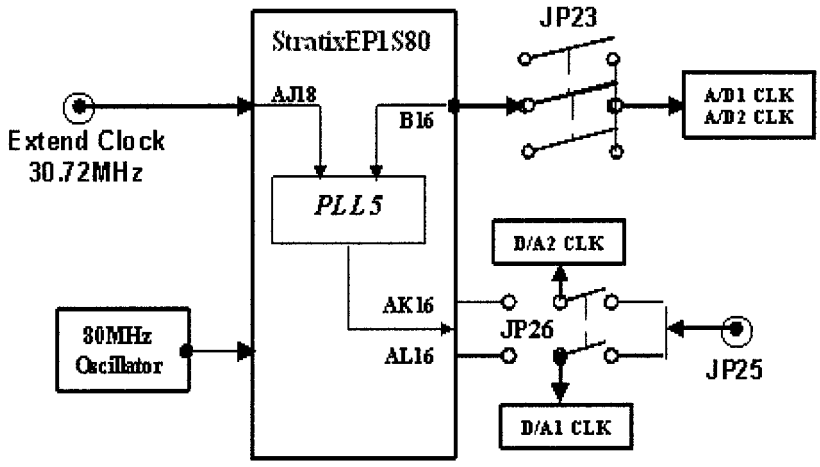

Figure 4- 3 Clock distribution diagram

Figure4-3 shows the clock distribution. D/As and A/Ds clock is provided by the PLL inside the FPGA. It is a four times the input clock.

4.2 The Implementation of the Digital Demodulator

4.2.1 Introduction and theory of the DDEM implementation

Baseband filtering and IF demodulation can be done in digital domain, due to the improvements in speed of data converters and programmable hardware technology. There are several advantages of implementing the DDEM design in the digital domain using digital signal processing board:

- Affords greater flexibility and higher performance in terms of attenuation and selectivity.
- Offers better time and environment stability than traditional analog techniques.
- High-speed components available make DSP, which extends from baseband processing to intermediate frequencies processing, and useful for tuning signal selection, frequency up- and down- conversion.

The IF signal is fed into the A/D input. For multi-carrier W-CDMA applications, if the one-channel signal bandwidth is 3.84MHz, then the three-channel signal bandwidth is 3*5 MHz (including guard bands). The predistorter attempts to add 3^{rd} order intermodulation products to the input signals in a way that cancels out 3^{rd} order intermodulation products added by the PA. Thus, the bandwidth of the predistorted output signal must be three times greater than the bandwidth of the original signal, which represents 3^{rd} order intermodulation products. Non-linearity effect which comes from spectrum regrowth at the PA output is three times basic band, so the total IF signal

bandwidth with nonlinear information of the PA is $BW = 3*3*5 = 45MHz$.

The analog-to-digital conversion at the output of the PA is traditionally done with input Nyquist rate in order to avoid the aliasing at the output spectrum. Figure4-4 shows the concept of the input Nyquist sampling rate in the IF input. The input Nyquist rate is the sampling frequency when the highest frequency of the input signal coincides with the lowest frequency of the image signal [26].

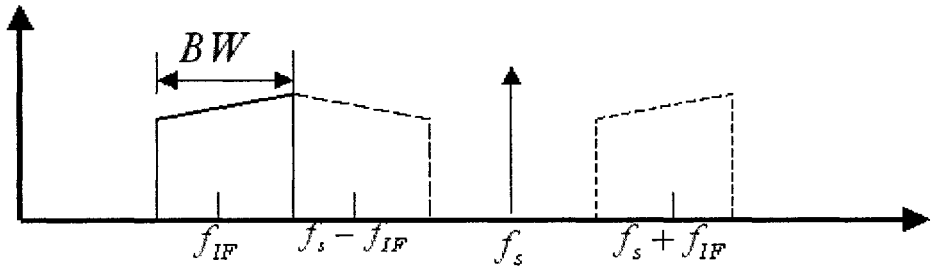

Figure 4- 4 Input Nyquist sampling rate concept in the frequency domain

$$f_{IF} + BW/2 = f_s - f_{IF} - BW/2$$

$$f_s = 2f_{IF} + BW \tag{4.1}$$

Assume $f_{IF} = 30.72MHz$, $f_s \geq 2*30.72 + 45 = 106.44MHz$

The sampling clock used in the DDEM is:

$f_s = 4*30.72 = 122.88MHz$ $\qquad$ $f_{IF} = 30.72MHz$

The wideband IF signal is translated to a complex baseband signal by quadrature multiplication. The NCO generates the quadrature sinusoidal signals for the multipliers.

The complex baseband signal is passed through low pass filter to prevent aliasing due to harmonic frequencies. Figure4-5 shows the functional block diagram of a single channel digital demodulation.

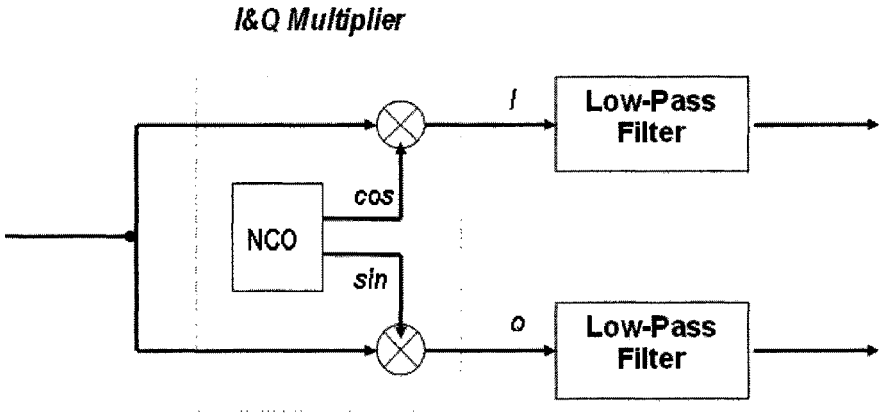

Figure 4- 5 Digital demodulator functional block diagram

The digital demodulator comprises of an NCO sinusoidal signal generation unit and two multipliers. The input signal real data is split into Q components and I by multiplication with a sine and cosine waveform. The outcome is a signal with reduced amplitude and two frequency components generated for both Q & I data streams. These streams contain the baseband signal and a secondary signal located at $2f_{IF}$. (f_{IF} is the IF carrier frequency). The secondary signal is removed after filtering.

The following equations describe the result of the Q/I splitting and multiplication operation in the frequency domain. (Input signal x (t))

$$\cos(w_{IF}t)x(t) \leftrightarrow 0.5X(w - w_{IF}) + 0.5X(w + w_{IF}) \quad (4.2)$$

$$\sin(w_{IF}t)x(t) \leftrightarrow 0.5X(w - w_{IF})j + 0.5X(w + w_{IF})j \quad (4.3)$$

4.2.2 The implementation of the digital demodulator using the FPGA

The digital demodulator design is optimized using the Altera Stratix EPS1S80B956C6 devices. The design employs two Altera intellectual property (IP) cores: finite impulse response (FIR) compiler and numerically controlled oscillators (NCO) compiler.

The Numerically Controlled Oscillator (NCO) is created using the Altera NCO Compiler MegaCore function. The NCO clock frequency is 122.88MHz. The output frequency is 30.72MHz, which generates both the sine and cosine waveforms for Q and I channel [18] [19].

The NCO implementation accounts for considering several parameters like: spectral purity, frequency resolution, performance, and throughput and device resources.

1. Spectral purity

The spectral purity of an oscillator is measured by its signal-to-noise ratio (SNR). The SNR is a measure of the signal power relative to unavoidable quantization noise inherent in its discrete-valued representation; it is a direct result of the finite precision with which NCO represents the output sine and cosine waveforms. Increasing the output precision results in an increased SNR, the following equation estimates the SNR of a given sinusoid with output precision b:

$$SNR = 6b - 1.8(dB) \tag{4.4}$$

Each additional bit of output precision leads to an additional 6dB in SNR. An 18bit magnitude precision is chosen for our NCO. So the total SNR is 106.2dB

2. Maximum output frequency and frequency resolution of the NCO

The maximum frequency of sinusoid that NCO can generate is bounded by Nyquist criterion to be half the operating clock frequency. Given the input clock rate, the maximum output frequency is $f_{\max} = \frac{1}{2} f_{clock} = 122.88/2 = 61.44MHz$.

The NCO outputs a sinusoidal waveform in two's complement representation; the waveform for the generated sine wave is defined by:

$$s(nT) = A * \sin[2\pi(f_0 + f_{FM})nT + \phi_{PM}] \tag{4.5}$$

- T: The input clock period T = 8.138ns
- f_0: The unmodulated output frequency based on the input value ϕ_{INC}, $f_0 = \frac{\phi_{inc} f_{clock}}{2^M} Hz$, M is the accumulator precision, if we create f_0 =30.72MHz, with M = 31bits, then $\phi_{INC} = 0.25 * 2^M = 536870912$
- f_{FM} : Frequency modulating parameter based on the input value ϕ_{PM}, ϕ_{PM} =0
- ϕ_{PM} : The phase modulation input value, $\phi_{PM} = 0$
- A: 2^{N-1} where N is the magnitude precision, $A = 2^{18-1} = 131072$

The minimum possible output frequency waveform is generated for the case

where ϕ_{INC} = 1, so the frequency resolution of the NCO is $f_{res} = \frac{f_{clock}}{2^M} Hz$ = 0.05722Hz

Table 2 shows the parameters employed in NCO Compiler. The built-in spectral plotter display shows that this selection of the parameter gives better spectral performance.

Table 2 NCO Compiler setting

Parameter	Setting
Generation Algorithm	Multiplier Based
Accumulator Precision	31
Angular Precision	16
Magnitude Precision	18
Implement Phase Dithering	On
Dither Level	Set to the middle of the slider bar
Phase Modulation Input	On
Frequency Modulation Input	Off
Outputs	Dual Output
Target Device Family	Stratix
Multiplier-Based Architecture	Use Dedicated Multipliers
Clock Cycles per Output	1

The digital demodulator employs a FIR filter to filter out the image frequencies. The filter is created with the Altera FIR Compiler MegaCore function. The FIR Compiler Wizard automatically generates floating-point filter coefficients, performs floating-point to fixed-point conversion, and generates a FIR filter in hardware. The desired filter is a low pass filter with a cut off frequency at 15.36MHz (a one-channel signal bandwidth of

3.84MHz with 3rd and 5th order intermodulation products) and an input sampling rate of 122.88MHz.

1. Specify the coefficients

A FIR filter is delimitated by its coefficients. The FIR Compiler coefficient generator, which supports a variety of filter types, creates the coefficients automatically. A 45 tap Blackman filter is used.

2. Analyzing the coefficients

The coefficient analysis tool is used in the FIR Compiler to scale precision of the coefficients. A signed binary fractional number has format:

«Sign» «Integer bits». «Fractional bits»

A signed binary fractional number is interpreted as an equation below:

Original input data: «Sign» « x_1 integer bits». « y_1 Fractional bits»

Original coefficient data: «Sign» « x_2 integer bits». « y_2 Fractional bits»

Full precision output data: «Sign» « I integer bits». « $y_1 + y_2$ Fractional bits»

I = ceil (log2 (number of coefficients)) + $x_1 + x_2 + 1$

A bit width of 16 was chosen in the coefficient specification area.

Because each value of the coefficient is between –1 and 1, we get = 0, = 15.

3. Specify the I/O number formats and bit widths

The input data is 14 bits and has a fraction format, so $x_1 = 0$, $y_1 = 13$.

A full resolution was chosen for the output data scaling. The FIR Compiler calculates the total number of output bits required for full resolution based on the bit width of the coefficients, it is: I = ceil (log2 (45) + 0 + 0+1 = 6, $y_1 + y_2 = 13 + 15 = 28$.

The full output resolution bit is 35 (D34...D0).

If the output has limited precision 14 bits (A13...A0) then one has to truncate 4 bits from the MSB, and round 17 bits from the LSM.

D34 _____ Remove

...

D30 _____A13 (MSB)

D29 _____A12

... ...

D17 _____A0 (LSB)

D16 _____Remove

...

D0 _____ Remove

The implementation architecture we selected is a fully parallel filter. It creates a fast filter (140 to over 300 MSPS) throughput with pipelining.

Table3 shows the parameters settings employed in the FIR Compiler wizard. Figure4-6 displays the FIR Compiler coefficient analysis page. The filter has the attenuation ratio of 80dB of the assigned frequency to the rejected frequency.

Table 3 FIR low-pass filter parameters setting

Parameter	Setting
Sample Rate	122.88 MHz
Filter Type	Low pass
Cut-Off Frequency	15.36MHz
Window Type	Blackman
Number of Taps	45 taps
Coefficient Scaling Type	Signed Binary Fractional
Coefficient Bit Width	16 bits
Input Bit Width	14 bits
Output Resolution	Full Precision
Architecture	Fixed Coefficient Fully Parallel
Pipeline Level	1
Data Storage	Auto
Coefficient Storage	Logic Cells
Simulation Models Generated	Matlab

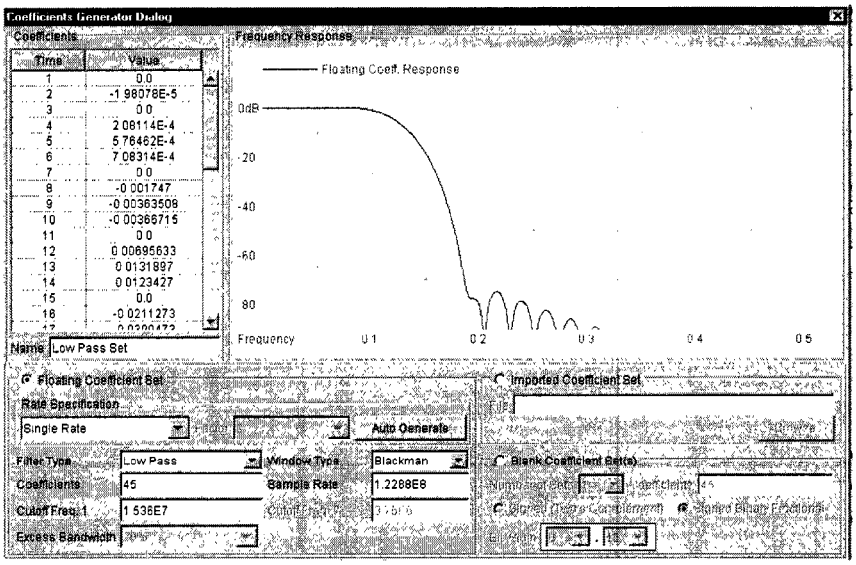

Figure 4- 6 FIR Compiler coefficient analysis page

The block diagram of the DDEM design using QuartusII software is shown in figure4-7. The Reformat block transforms signed notation to an unsigned one as the DAC is expecting an unsigned data format.

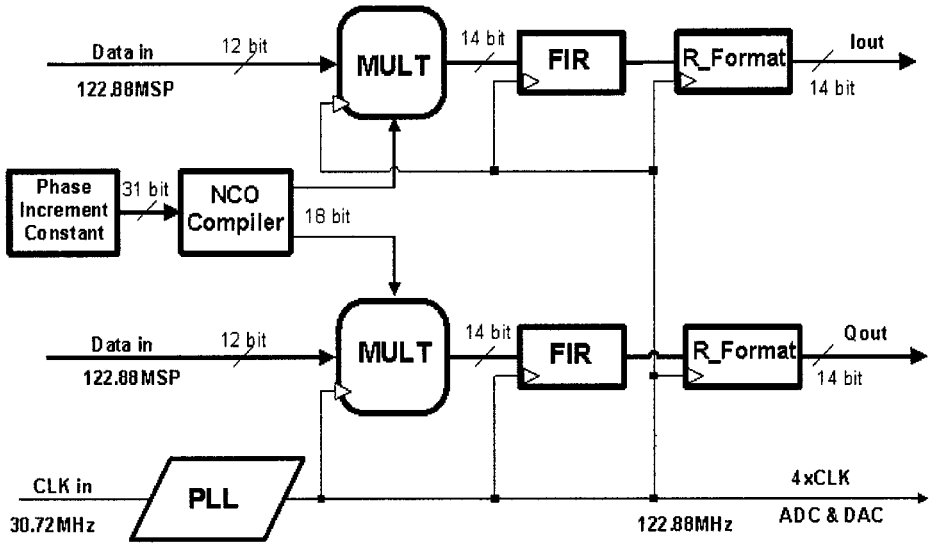

Figure 4- 7 The design of the digital demodulator in QuartusII

The implementation of DDEM employs two multiplications at 122.88MHz. The multiplier muliltplies the IF input data of 14 bits and the NCO input data of 18 bits, which results in a limited precision output of 14 bits.

4.2.3 Measurement results and analysis of the DDEM design

The test set up is shown in figure4-8. A Vector Signal Generator SMIQ-B47 with a Dual-Channel Modulation Generator AMIQ was used as a signal source, which generates W-CDMA modulated signals.

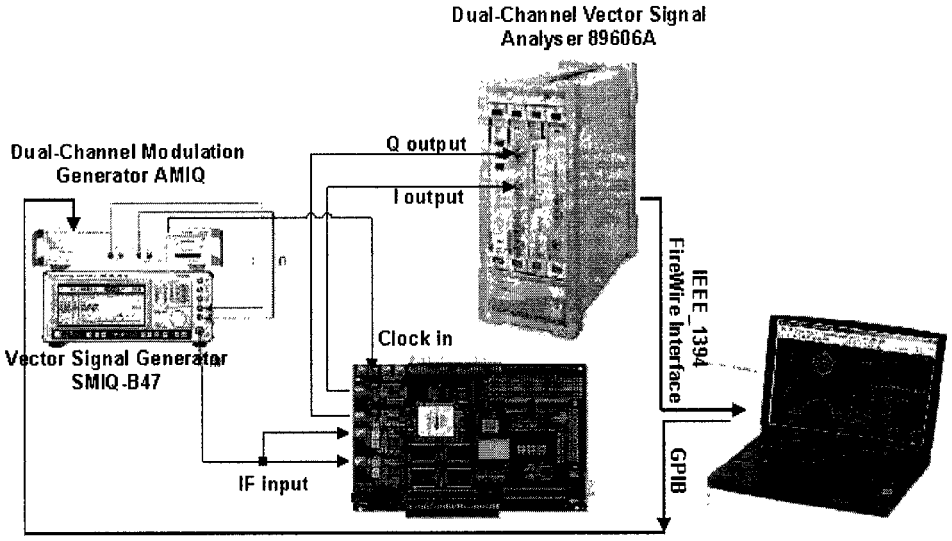

Figure 4- 8 Testing block diagram of DDEM design

A CDMA-2000-SR3 signal is first synthesized with the ADS CDMA2K library, then this signal is uploaded to the AMIQ, the up-converted output signal of the SMIQ with IF = 30.72MHz is fed to the DDEM (Input ADC1 and ADC2 in DSP Development Board). An external clock at 30.72MHz is used for synchronization at connector JP3 of the DSP development board. The sampling clock of the ADC and DAC is four times PLL input clock (30.72MHz*4=122.88MHz) in the FPGA design. The QuartusII software creates .sof programming design file for the DDEM, which is downloaded to FPGA. The demodulated analog output signal of the DDEM from DAC1 (I) and DAC2 (Q) is fed to the two baseband channels of the Vector Signal Analyzer (VSA) 89606A. A laptop was used to run the WinIQSIM &ADS software and the vector signal analysis software for the acquisition of the dual-channel baseband waveform signals. It also captures the complex modulated signals at the output of the dual-channel DDEM.

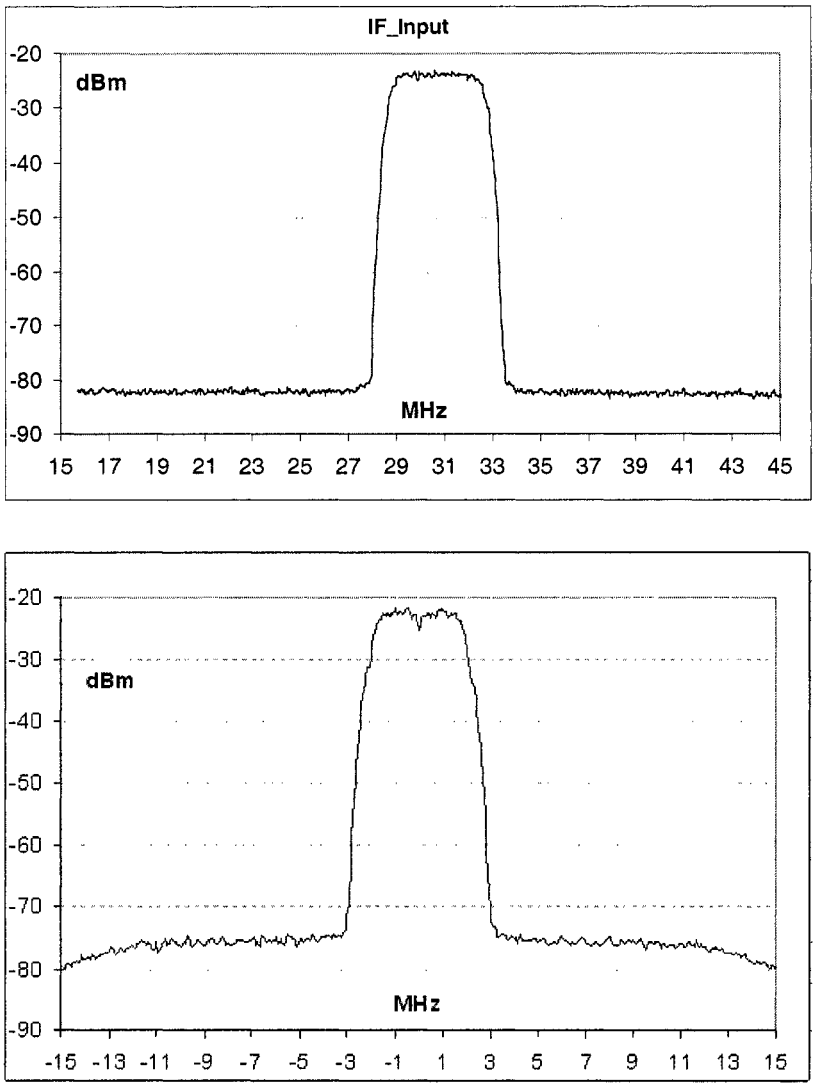

Figure 4- 9 Measurement results of DDEM in frequency domain

Several measurements were made and the testing results are shown in Figure4-9. The tested signal is a single carrier W-CDMA signal. The first plot is the input IF signal with center frequency at 30.72MHz, and PAPR is 56dB with power level –25dBm. The second plot is the output of demodulator after low pass filtering, the extra noise and

harmonic component has been removed by filtering, the output PAPR and power level of the demodulator keeps the same characteristics with input signal, it means the demodulator has perfect intermodulation performance and channel selectivity due to the higher rejection ratio of the digital filter.

4.3 *DPD Implementation*

4.3.1 Introduction of DPD implementation

The DPD implementation block diagram using a LUT is shown in Figure4-10.

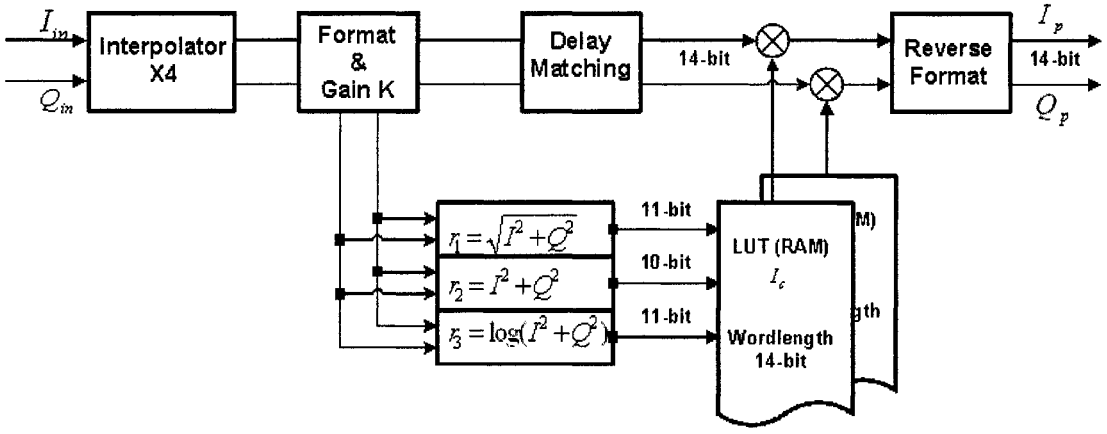

Figure 4- 10 DPD implementation block diagram

The input is 14 bits of unsigned baseband data stream I_{in} and Q_{in}, and has sampling rate of 30.72 MSPs. The interpolation filter is used to increase sample rate, which increases the output sample rate by a factor of 4. It generates 122.88MSPs of over sampled data stream. By increasing the input the sampling rate, increases the new

Nyquist frequency so that the spacing between the desired signal and the alias is also higher. It relaxes the roll off requirements of the anti-aliasing filter, and also relaxes the requirements of the analog low pass filter at the output of the DAC.

If the LUT address is derived from the equation $r = I_{in}^2 + Q_{in}^2$, the index of the table has to compensate for the unmatching between r and envelope power level with a correcting coefficient. In the design, logic operation data format is fractional two's complement. The format function and reverse format function are used to convert the input unsigned data stream to signed.

If one utilizes the different index of LUT, the change in the design is the Address Calculation block and the data value saved in the LUT too.

The address width of the table is 11 bits, which can index 2048 bits of memory. The initialization file of the table is saved in dual-port RAM. The word length of the LUT contents is14 bits. There are two tables $r \rightarrow I_c$, and $r \rightarrow Q_c$. DSP Processor updated the content of RAM using data write port.

The Delay Matching block delays the input data. Prior to undergoing a complex multiplication, the elaborate delay matching compensates for the delay of the signal traveling through the address calculation, indexing table, and reading out of data from the LUT. This takes about 3 clock cycles.

The correcting data is added to the original data using the complex multiplication, which written as:

$$I_p + jQ_p = (I_{in} + jQ_{in})(I_c + jQ_c) = (I_{in}I_c - Q_{in}Q_c) + j(I_{in}Q_c + I_cQ_{in})$$

$$I_p = I_{in} I_c - Q_{in} Q_c \tag{4.6}$$

$$Q_p = I_{in} Q_c + I_c Q_{in} \tag{4.7}$$

4.3.2 The implementation of DPD using the FPGA

Altera Stratix device has dedicated digital signal processing blocks. It efficiently implements multiplication and multiply accumulation (MAC). A single DSP block can be configured as four 18x18 bits multipliers. A single DSP block (mode 18*18 bit) implements a Vector Multiplier and an Address Calculation. The real part calculation $I_p = I_{in} I_c - Q_{in} Q_c$ uses one multiplier subtraction/accumulator and the imaginary part calculation $Q_p = I_{in} Q_c + I_c Q_{in}$ uses another multiplier adder/accumulator for 14 bits data bus. The calculation of address $r = I_{in}^2 + Q_{in}^2$ uses one multiplier adder/accumulator too.

The design is synchronized. The operation feeds a pipeline register. Each pipelined operation building block utilizes one clock cycle to obtain each computation result. Pipelining is useful for the performance improvement over equivalent functionally combination design. Another advantage of pipelined design is the increased data throughout. To obtain the first result employed initial clock is called the latency of the pipelined design. The total latency of logic operation is 4 clock cycles in design.

The QuartusII top-level design is shown in figure4-11. LUT and V_MULT is the sub-design of Look-Up-Table and Vector Multiplier. 4XFIR is 4-time interpolation filter,

which upsamples input data from 30.72MSPs to 122.88MSPs. The input 14 bit data Q and I come from data interface header JP8 and it passes through a Format block. The Format block transfer unsigned to sign also multiplies gain coefficient. The output data from Format block is up sampled to 122.88 MSPs using Block X4FIR. The upsampled data is delayed and multiplied with LUT correction data using V_MULT block. The14-bit Data_in Bus and 10-bit Write Address update the LUT data.

The output data from V_MULT is first pass through a FIR filter with the correcting function $\frac{x}{\sin x}$. It corrects the Digital to Analog Converter (DAC) frequency characteristic $\frac{\sin x}{x}$. Finally it is converted to unsign by block Reformat. PLL is a digital Phase Locked Loop; it provides the global clock and clock of the DAC.

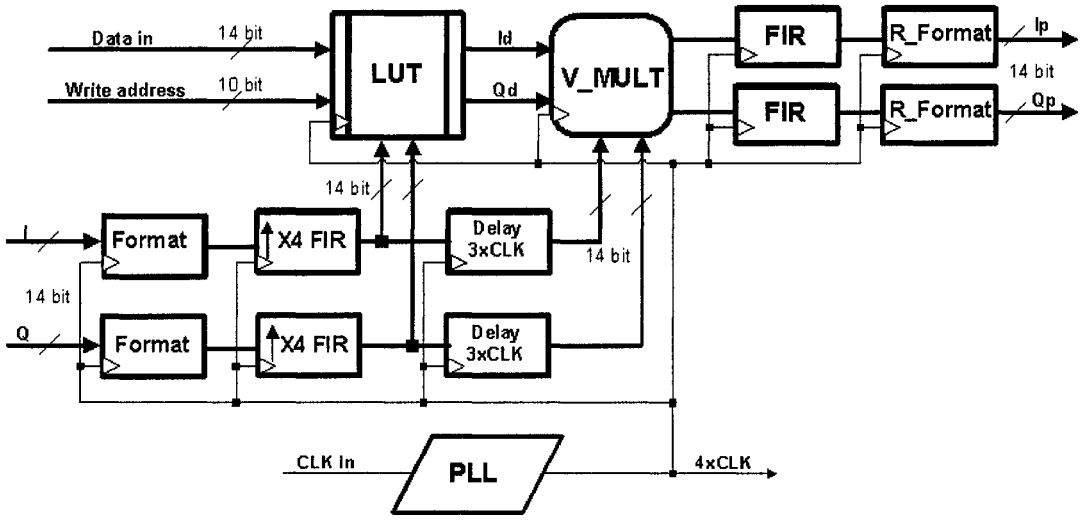

Figure 4- 11 The top-level design of DPD in QuartusII

The following discussion is the detail design procedure of each block.

Look-Up-Table Subdesign

The look-up-table subdesign includes a table address calculation block and two tables; which is built using the dual-port RAM (2*2048bits).

The table address calculation block uses the multiply accumulator. The output of the multiplier stage feeds the adder/output block, which is configured as an accumulator. The input bus is 14 bits wide. The full precision output has 2*14=28 (27...0) bits.

The table memory uses a parameterized dual-port RAM Megafunction, and the parameter settings of the dual-port RAM are listed:

Table 4 DP-RAM setting of LUT

Port Name	Description	Setting
Data	Data input to the memory	14-bit
rdaddress[]	Read address input to the memory	11-bit
wraddress[]	Write address input to the memory	11-bit
Wren	Write enable input.	1-bit
In clock	Positive-edge-triggered clock.	122.88MHz
q[]	Data output from the memory	14-bit

The initial contents of the table are saved in RAM as a memory initialization file. The file is an ASCII text file (with the extension .mif). Two tables are required for each memory block Q and I. Each memory has depth 2048 and word width 14 bits. Using port wraddress[] and data[] updates the contents of the table.

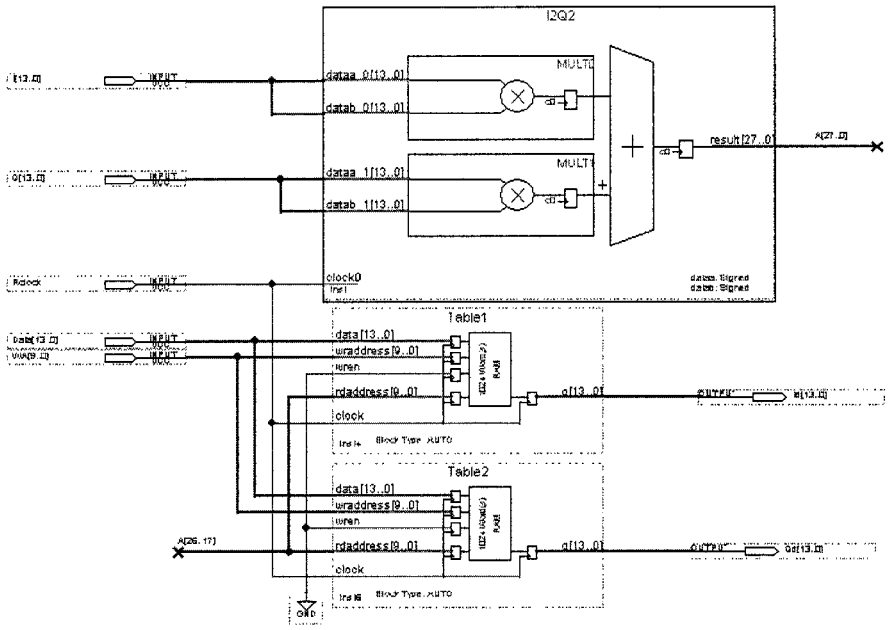

Figure 4- 12 The sub- design of LUT in QuartusII

Vector multiplier

Two multiplier accumulators implement the Vector Multiplier subdesign. One DSP block built by two multiply accumulator with sums and differences (four 18-bit X 18-bit), calculates the real part $I_p = I_{in}I_c - Q_{in}Q_c$ which uses one multiplier subtraction/accumulator, the imaginary part $Q_p = I_{in}Q_c + I_cQ_{in}$ uses another multiplier adder/accumulator. The output of the two blocks is full-precision 29 (28...0) bits. We scaled the output to a limited precision of 14 bits. The output signal is registered by output port.

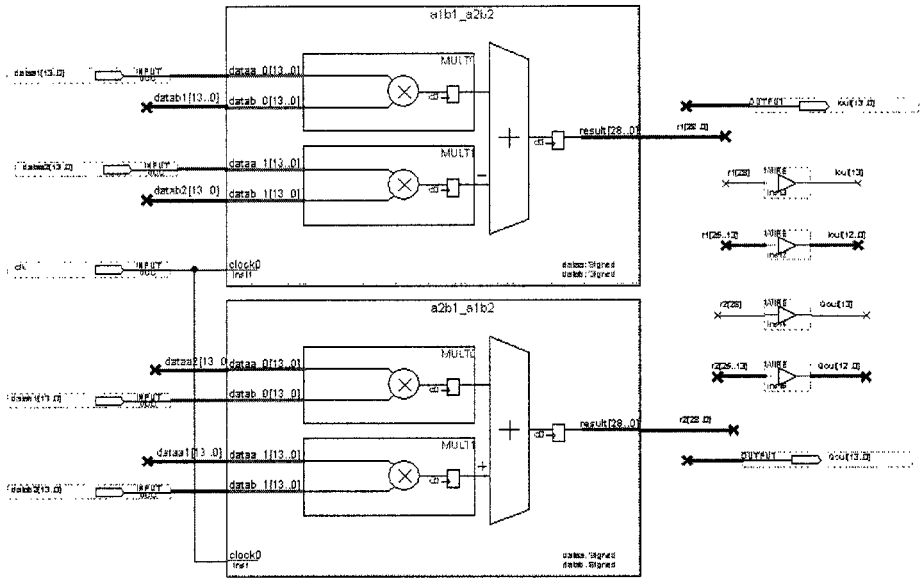

Figure 4- 13 The sub- design of vector multiplier in QuartusII

Interpolator

Figure4-14 shows the time and frequency domain representation of interpolation. Assume the input signal spectrum is limited to 15MHz (3 carrier W-CDMA), and the interpolation factor is 4. Interpolator increases the output sample rate by a factor of 4 by the insertion 3 zeros padding between the input samples. This upsamples input data from 30.72MSPs to 122.88MSPs. Inserting zeros creates reflections of the original spectrum, and a low pass filter is needed to filter out the reflections.

The four times rate interpolation is performed in two steps (figure4-15): upsampling and quarter band filtering. The interpolator filter is implemented with polyphase architecture by using the multi-cycle variable architecture of the FIR Compiler v3.0. Polyphase interpolation filters provide the following benefits:

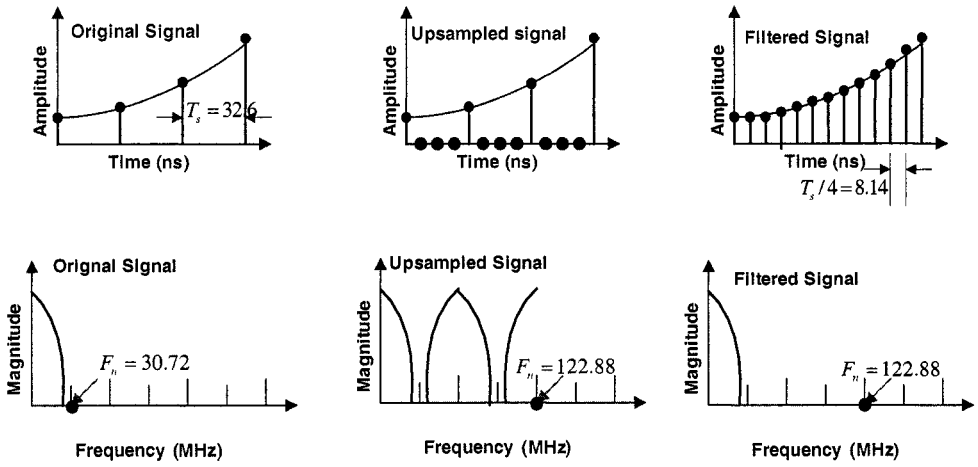

Figure 4- 14 Time & frequency domain representations of interpolation 4X

- Speed optimization – each of the polyphase filters runs at the input data rate, it reduces the number of computations required per cycle, and it means increasing the throughput of data.
- Area optimization – The polyphase interpolators shares resource.
- Less group delay – The polyphase architecture takes 1/I group delay.

Assuming the length of the FIR filter is 44 taps with an interpolation factor of I=4, the polyphase implementation splits the original filter into 4 polyphase filters with 11 tap lengths. The number of channels and the coefficient set is 4. If the original filter impulse response is $h(n)$, then the polyphase filter response is $h_m(n) = h(m+nI)$, m=0, 1, 2, 3. The output representation of interpolator with interpolation factor of 4 is given by:

$$y(n) = \sum_{i=0}^{43} h(n-4i)x(i) \tag{4.8}$$

In order to implement a multirate FIR using polyphase decomposition targeting

the MCV architecture, one used the multi-channel, multiple coefficient set configuration to mimic the polyphase decomposition structure. It is necessary to add a counter, which feeds into the coef-set port. The number of channels and the number of coefficient set is dependent on the interpolation factor.

With an interpolation factor of 4, the filter has four polyphase outputs. Each output is considered as one of the polyphase outputs, and running at the input data rate, the input should be held for 4 clock cycles.

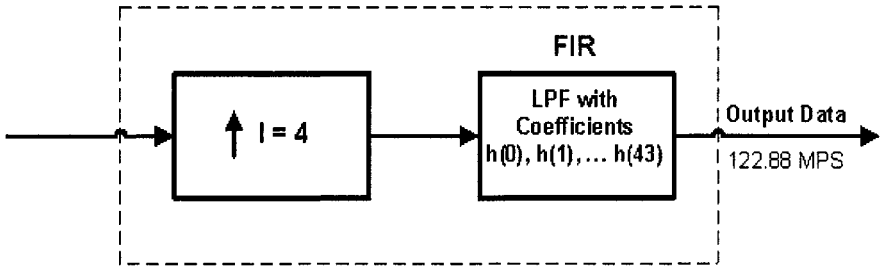

Figure 4- 15 Interpolation architecture using lowpass filter

Table 5 Coefficient bank of Interpolation filter

Filter Bank	Coefficients
Coefficient Set #1	h(0), h(4), h(8), h(12), ... h(36), h(40)
Coefficient Set #2	h(1), h(5), h(9), h(13), ... h(37), h(41)
Coefficient Set #3	h(2), h(6), h(10), h(14), ...h(38), h(42)
Coefficient Set #4	h(3), h(7), h(11), h(15), ...h(39), h(43)

First we separate the 44-tap coefficient set into 4 filter banks based on the decomposition shown in Table5. Each coefficient set consists of 11 coefficients with a text file. When reloading the coefficients, we use the New Coefficient Set, select

Imported Coefficient Values from the Coefficient Generator Dialog box, and indicate the coefficient set accordingly.

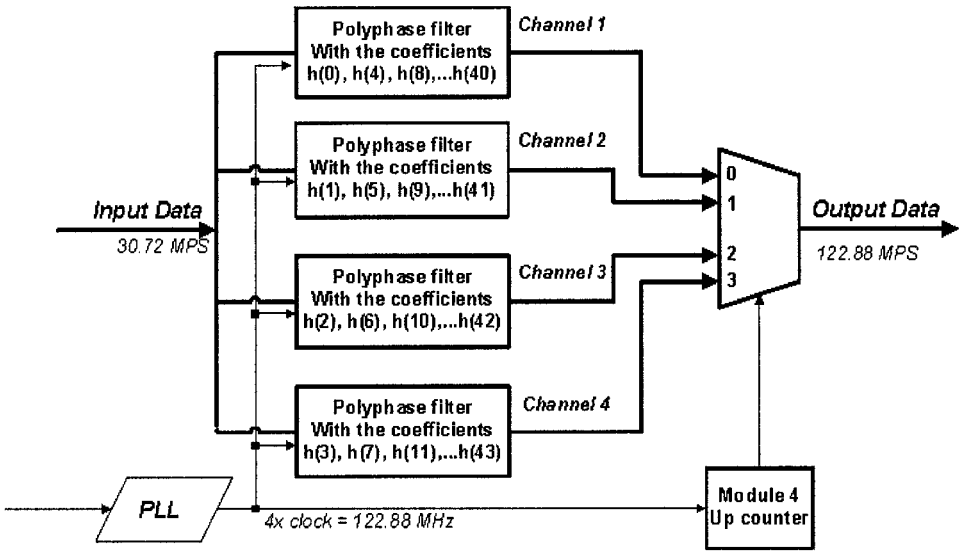

Figure 4- 16 Implementation block diagram of polyphase upsampler

Table 6 Parameters setting of upsampler

Parameters	Value
Input data bit width	14
Coefficient bit width	16
Number of coefficient sets	4
Number of channels	4
Architecture	Variable/Fixed Coefficient: Multi-Cycle
Data storage	Logic Cells
Coefficient storage	Logic Cells
Multipliers	DSP Blocks
# Cycles to compute	1

The FIR Compiler block is optimized for throughput, and the parameters settings of the upsampler in FIR Compiler v3.0 is shown in table 6. Figure4-17 shows the design schematic in QuartusII with the FIR Compiler for multiple coefficients sets the configuration for the polyphase decomposition structure.

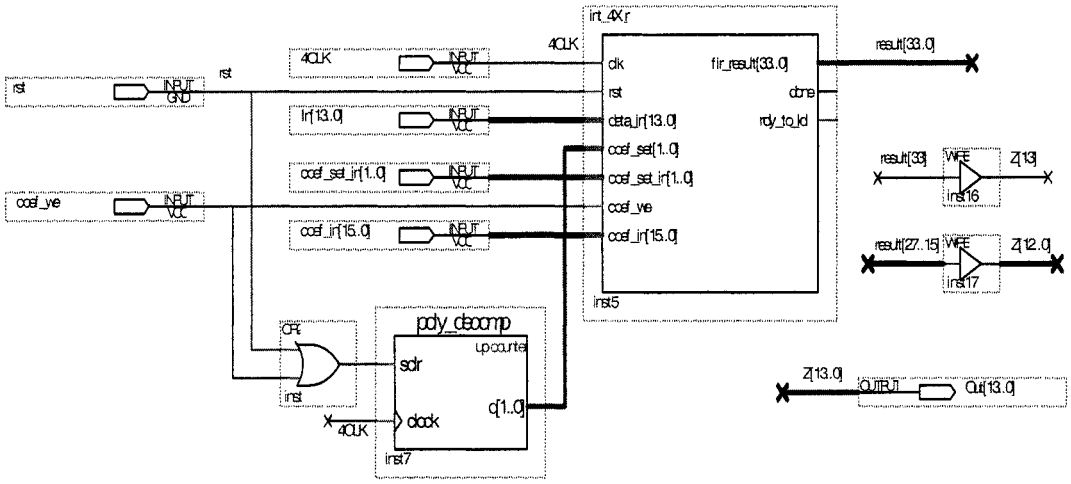

Figure 4- 17 Design of polyphase interpolator

The interpolation effectiveness is tested in frequency domain. We used the test bench (shown in figure4-18), interpolated signals both Q and I at the output of DACs are modulated using Vector Signal Generator at the frequency = 1.96GHz. A W-CDMA baseband signal is used for testing. The output signal in frequency domain was captured using Agilent E4440A Spectrum Analyzers.

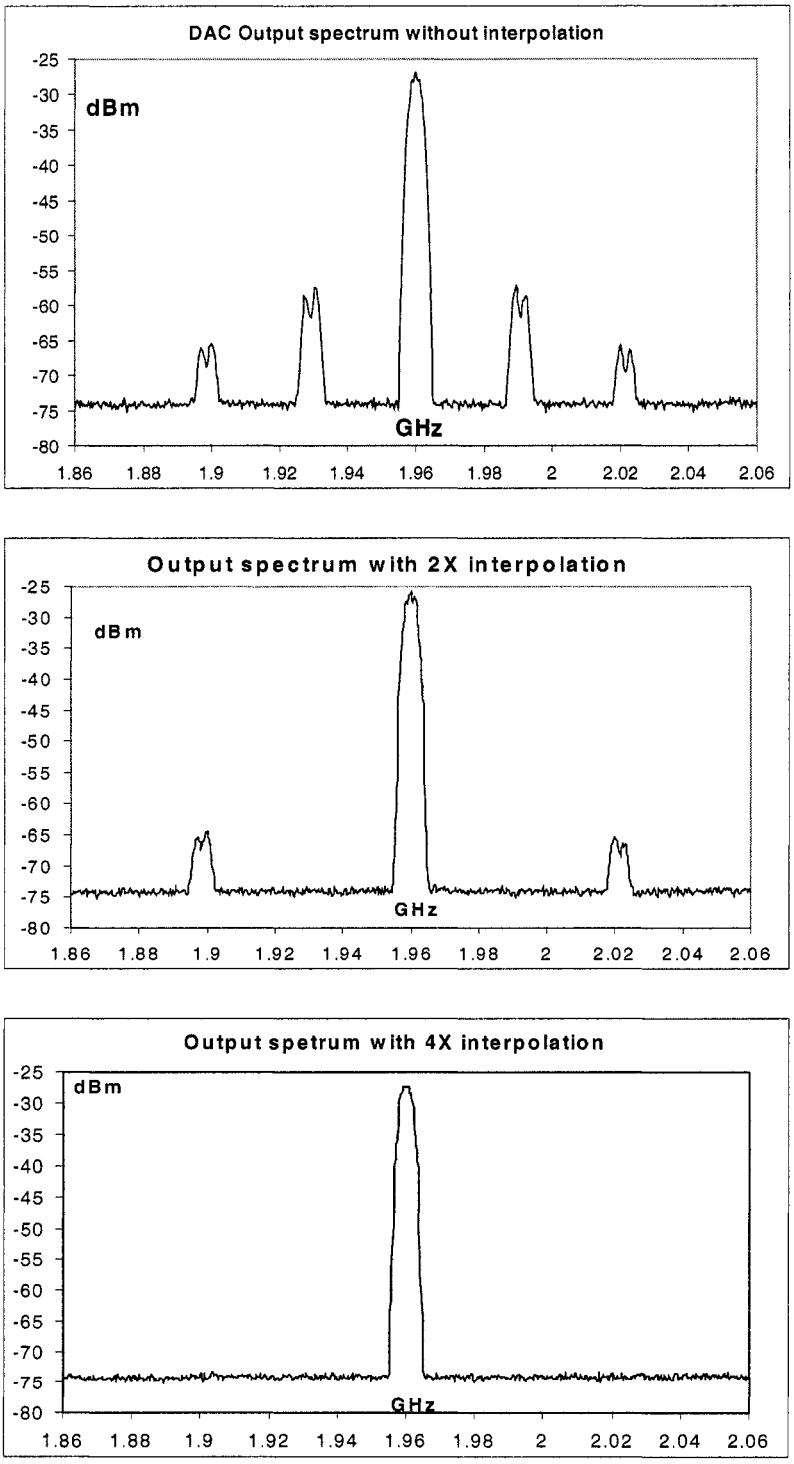

Figure 4- 18 Spectrum of interpolation effeteness

The output spectrums of the D/A converter consist of fundamental and harmonics at a frequency of $\pm I * 30.72MHz$ (I is the interpolation factor). It is clear that increasing sample the rate results in a higher spacing between the fundamental signal and its harmonics. In Figure4-21, the first plot is the spectrum without interpolation, and there are harmonics at frequency (n=1, 2...) when the input data stream of DAC is 30.72MSPs. The second pane is the spectrum of signal after two times interpolation, the sampling rate of the DAC being 61.44MHz. It is obvious that after 2-time interpolation, the sampling rate increasing two times, the harmonics component is increased at $\pm n * 61.44MHz$. The third plot is the spectrum of signals after 4-time interpolation. The DAC works at a sampling rate of 122.88MHz, and the harmonic is $\pm n * 122.88MHz$.

4.3.3 Measurement and results analysis of DPD

The DPP testing set-up is shown in figure4-15. A Dual-Channel Modulation Generator AMIQ is the signal source, which creates the digital baseband signal and synchronized clock. The synchronized clock at 30.72MHz is used for external clock (JP1) source of the DSP development board. The sampling rate of the input signal is 30.72MSPs. Both Q and I have the format of 14 bits unsigned. A Vector Signal Generator SMIQ-B47 is used to upconvert the predistorted signal to RF. Agilent E4440A PSA Series Spectrum Analyzer is used to capture the output spectrum of the SMIQ.

One figure is the spectrum of the LUT with the table content $I_c = 1$ and $Q_c = 0$, using equation (4.6) (4.7): $I_p = I_{in} I_c - Q_{in} Q_c = I_{in}$, and $Q_p = I_{in} Q_c + I_c Q_{in} = Q_{in}$.

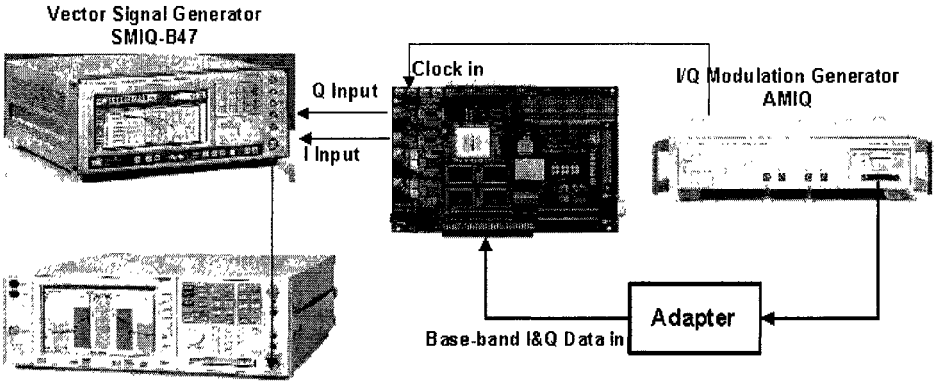

Figure 4- 19 The testing block diagram of DPD implementation

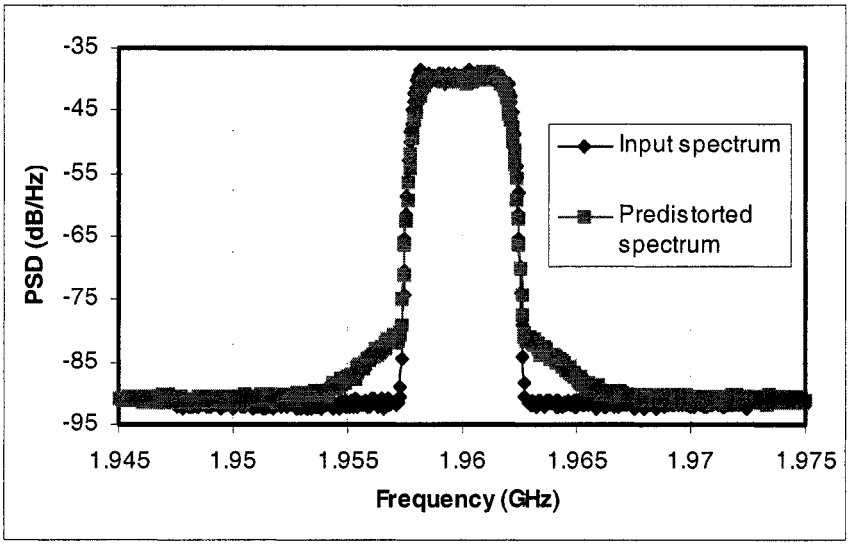

Figure 4- 20 The measurement results of the DPD design

The other one is the predistorted signal spectrums with index function $I^2 + Q^2$. We can observe that the signal resembles the predistorted spectrum with nonlinear behavior of a PA with the reverse phase, we got the expected predistortion effectiveness coincides with the simulation results in Matlab (figure2-5).

Chapter 5: Conclusion and Future Work

Conclusion

The design and implementation of an adaptive baseband digital predistorter, which is suitable for linearizing a RF power amplifier for 3G base station application, using LUT has been discussed. The system developed includes an FPGA-based predistorter, a digital demodulator, and a RF receiver (mixer + IF amplifier).

Analog device AD8343 and AD8370 were used to design the active mixer and the digitally variable gain IF amplifier respectively. The active mixer and the IF amplifier were designed with a flexible and balanced implementation architecture. They provide high performance (low intermodulation and anti-noise), high conversion gain, and low LO drive level. Near perfect symmetry of the circuit layout results in low RF and LO leakage. The measurement results illustrated more than 20dB gains, 61.3dBc intermodulation performance.

By means of fast A/D, D/A converter, high speed FPGA, Altera intellectual property (IP) cores, our DPD and DDEM have:

1. Provided wider bandwidth due to high speed processing capability
2. Afforded greater flexibility due to block, multi-level architecture design mode
3. Offered higher performance due to bit precision resolution

The digital predistorter was implemented using Altera Stratix EPS1S80B956C6 device. The design was validated using Altera Stratix DSP development board. The measurement results of both frequency- and time-domain demonstrated the effectiveness

of the predistortion when driven by 3G signals, which coincide with simulation results in Simulink (Mathworks).

Future work

1. Apply the design to the system in order to validate the effeteness of predistorter.

2. Utilize higher speed A/D Converter to digitize the two outputs of the mixer in order to minimize the quantization noise.

3. Use other indexation method of look up table: Indexing with the amplitude of input signal ($\sqrt{I^2+Q^2}$) leads to equal spacing of LUT entries, index with logarithmic companding functions $\log(I^2+Q^2)$ and another companding function that takes into account the variation of signal statistics and the operation power backoff point.

4. Take into account of the memory effect compensation of PAs.

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